QUANTUM TECHNOLOGY, INC.

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INSTRUCTION MANUAL
FOR
MODEL
HVP-5I-DIFF-5
W/QS-3-2H

SN:E02-159

HVP-5I-DIFF DRIVER OPERATIONS MANUAL

WARNING: ALL SAFETY PRECAUTIONS MUST BE OBSERVED.

UNPACKING INSTRUCTIONS

1. Check the package for damage before accepting it. If possible, refuse badly damaged packages. Notify the carrier as well as Quantum Technology, Inc.

2. Check the contents of all packages against the packing slip. Missing items will be replaced immediately by Quantum Technology, Inc.

INSTALLATION

INITIAL INSPECTION:

If the shipping carton is damaged, ask the carrier's agent to be present when the system is unpacked. Check the electronics package for external damage such as broken or bent controls or connectors, and dents or scratches on the cabinet. Inspect the modulator for broken connectors or damaged windows. Check the performance of the system as soon as possible after receipt.

If damage is evident, notify the carrier and the nearest sales office. The sales office will arrange for repair or replacement of the system without waiting for settlement of a claim with the carrier. For other than initial inspection warranty claims, contact the sales office.

INPUT POWER:

The system was wired for either 100, 115, 208 and 230 VAC operation depending upon how the system was specified at the time of order. The rear panel label will indicate the input power that your system requires. The system is supplied with a three conductor power cable. The offset (round) pin on the power cable connector is the ground pin and it should be connected to a suitable ground.

GENERAL:

The HVP-5I-DIFF driver system uses the following components:

1 - HVP-590, -510, OR -595 Driver

1 - DVM display module

1 - HVPS high voltage supply which may be 50XX type (5 KV set, 6 KV internal limit) or 90XX type (9 KV set, 10 KV internal limit)

1 - DD1, DD1-1, or DD2 divider/delay for timing

1 - DIN5-DIN5-6' cable

1 - SHV-SHV-RG59-6' cable

The system is useful for Pockels cell shutters, mode locked pulse extraction and cavity dumping applications.

Additional cables maybe supplied for the specific hook-up diagram, which should be consulted.

HOOKUP CONNECTIONS:

Connect the system as shown on the cabling diagram included at the end of this section. After completing the connections, place the pockels cell in the optical path such that it is aligned with the laser beam. Use low power for safety when aligning the optical path. The system is now ready to be turned on.

INITIAL SETUP:

The following setup will produce a sample output and illustrates how the controls work. See the cabling diagram included.

1. Connect a TTL level pulse signal to each of the trigger inputs. The pulse source is usually the DD1 in the main chassis. The output pulse width will be the delta time between the two inputs, and either input can accept the leading trigger. The max pulse width is limited to approximately 3 usec. This is due to the inherent RC time constant droop rate governed by the resistor loads and total load capacitance in the unit. An optional high impedance output configuration allows pulse widths of more than one millisecond.
2. On the high voltage power supply turn the HV ADJ max counter clockwise. Press the "on" button to enable the high voltage.
3. At this time turning the HV ADJ clockwise will produce a high voltage pulse. The amplitude will be indicated on the panel meter in KV. This system will generate pulses up to a 8.1 KV max pulse level depending up on the options ordered. In some cases the output can be increased to 9 KV. Contact the factory for information.

DVM DISPLAY

The digital volt meter on the front panel is used to monitor important parameters within the system. When a module is selected by pushing the select button on its front panel, the meter will release any other module it is monitoring and switch to the selected module. For this system the DVM can monitor only the high voltage. When the button is pushed on the high voltage module, the meter is scaled to read the peak value of the high voltage pulse that will be produced when the system is triggered. This indicated value is usually less than the actual high voltage being generated by the high voltage supply.

MODEL 40SE-HVP HIGH VOLTAGE POWER SUPPLY

The 40SE-HVPS series plug in modules are high voltage power supplies consisting of a regulated low voltage power supply, a regulated high voltage power supply with associated control, and meter monitoring and switching circuitry. A 400 VDC bias output is also provided.

CONTROL AND OPERATION:

HVP Output: This is the high voltage output to the pulser. The load should be connected before turning on power to the system. The SHV connector on the HV output may arc if this is not done.

HV Adjust: This 10 turn dial sets the HV as displayed by the meter on the main power supply/meter plug in. This indicates the peak level of the high voltage output pulse.

HV Push Button: This push button toggles the HV ON and OFF as indicated on the front panel LED. When this push button is first depressed, the meter displays the HV set by the HV adjust, and the HV is ON. When it is depressed a second time the HV is turned off. This button has another purpose. If another plug in has selected the meter for its own display, depressing the button deselects the meter from that function and causes it to display the high voltage reading.

THEORY OF OPERATION:

This power supply consists of four sections. The first is the meter switching and high voltage enable and control circuits. The second is the high voltage supply, and the third is the 24 VDC supply that provides primary power to the high voltage supply. The four is the 425 VDC bias output. Refer to the schematic 21-547-F1K and the layout drawing 21-547-F400.

Meter Switching and High Voltage Enable and control:

The meter switching circuit works as follows: When front panel switch S1 is depressed, the meter buss line is connected to ground. This action disengages all other plug in modules from the meter, and both sets and presets one of the flip flops in U1 causing both output pins 5 and 6 to go high. It also produces a pulse through the capacitor C4 that toggles the other flip flops in U1 causing pin 9 to go low. This enables the high voltage as the analog switch, U2, pins 11 and 15 which are connected to the high voltage power supply remote input are now removed from ground and connected to the front panel "HV ADJUST" control.

On the release of S1, the first flip flop, which is being both set and reset, is left preset as the capacitor, C16, holds the preset voltage on pin 4 for a few msec after the set voltage on pin 1 had been removed. The same action controls the decimal point reading to show the correct decimal point position, DP2. This is

accomplished via U1 pin 6, Q bar output going low which also turns on the 10,000:1 HV sample (by output dividers R10 through R12) and directs that to the meter. R10 is the meter calibration adjustment. When the display switch is depressed a second time, U1 is clocked and toggles turning off the high voltage as pin 9 goes high. Pin 6 remains low keeping the meter connected to this function.

The 24 VDC power supply is a standard 115 VAC to 24 VDC chopper converter that supplies power to the high voltage supply. It comes on when the 40SE-PSM system AC switch is turned on.

This module accepts a variety of high voltage power supplies. They vary in output voltage from 3 KV to 10 KV and in output current from less than 1 MA to over 6 MA depending upon the system requirements.

The 400 VDC bias output consists of a rectifier diode, a filter capacitor, and a bleeder resistor. This produces a low current output that is used by the pulser trigger circuits.

MODEL DD1 DIVIDER DELAY UNIT

The Model DD1 Divider Delay Unit - The DD1 unit allows precise divider settings of 6 decades enabling MHz signals to be divided down to sub Hz rates. An alternate method of operation is to use the 6 decade settings to select precise pulse bursts counts out in both manual and external trigger modes. Programmed delays can also be generated. One of the more useful applications is dividing down mode lock signals to the rep rates required. The unit features high sensitivity for mode lock signals and two precise independent 1-99 nsec digitally settable delay outputs. One of the delayed outputs can be delayed up to an additional 900 nsec in 100 nsec steps. The unit can also be used as signal generator by operating it from its internal oscillator.

INSTRUCTIONS:

INPUT: The inputs are fed to the front panel through BNC connectors. On some special units, the input may be fed via BNC rear panel connectors. The input sensitivity is from 0.20 to 1 volt peak to peak so as to allow direct coupling to conventional pulse generators, mode lock signal sources, or even optically generated pick off signals.

INTERNAL/EXTERNAL MODE: This mode selects the master clock source, which is either the internal 250 MHz oscillator or an external input. External clock frequencies up to 240 MHz are accepted. Operation on the internal oscillator is the same as if the unit was operating on a 240 MHz external clock.

DIVIDER MODE: In the divide mode the six decade push button thumb wheel switches are utilized for setting the precise division required for the mode locked signal. The external clock is divided by 10 by a high speed scaler before entering the programmed divider which makes the division selected 10 more than is indicated by the front panel decade switches. Here the divider delay will produce three continuous outputs the direct output "ADV OUT", the delayed output "OUT 1", and the delayed output "OUT 2".

DELAY MODE: In the delay mode the unit will produce a pulse delayed from the "BURST" input or for a selected manual SS-BURST input by an amount equal to 10 times the six decade switch setting times the selected clock single cycle time. The OUT 1 and OUT 2 outputs are delayed additionally by their respective settings. The internal clock is equivalent to 240 MHz.

BURST MODE: In the burst mode the unit will produce a burst of "N" pulses for each pulse on the "BURST" input or for a selected

manual SS-BURST. The pulse count is equal to the number set on the six decade switches, and the output frequency is equal to the clock divided by 10. The OUT 1 and OUT 2 delayed outputs are also active but will not be useable if the delays selected exceed 5 times the clock cycle time. The positive edge triggered "BURST" input is TTL level compatible and capacitive coupled to a 50Ù load.

DELAY: The delay thumb wheel switches allow additional precise delay setting of the OUT 1 output up to 99 nsec and the OUT 2 output up to 999 nsec in one nsec increments. Up to 5 nsec additional continuously adjustable delay is also provided for each output. This is useful, for example, in setting the timing of a picked out pulse in a mode locked pulse train to coincide exactly at the precise time required when the appropriate pulse is at the correct optical path position in the modulator.

OUTPUT: All outputs of the delay unit are capable of driving approximately 3 volt peak to peak in to a 50 ohm load and are approximately 50 nsec wide. These outputs are TTL compatible, but high levels will reach approximately 7V peak if no other external loads are present.

THEORY OF OPERATION:

The clock input, via J2, is amplified by a gain of 7 through the high speed amplifier U11. U11 increases the sensitivity for optical pick off applications and for direct mode lock signal connections to conventional mode lock sources. The amplified signal out of U11 is fed to U2, which is a high speed divide, by 10 counter. This combination allows signals of up to 240 MHz to be accepted. The output of U2 is fed to the clock select logic where it or the internal 25 MHz oscillator becomes the source for the divider chain. This selection is made by the front panel INT/EXT switch (S11 on the schematic). The clock is fed to the first two counters of the six divide by 10 counters, U3 and U4, and to the mode select decoder U13. The Most significant bit (Q4) output of U4 is fed to U5 through U8 to become the clock for the remaining four counters. Pull up resistors on BCD switches S2 through S7 direct the selected BCD inputs to the divider chain for controlling the divide ratio, delay, and the burst count.

In the divide mode the decoded terminal count of the BCD counters at the output of U9 pin 6 is sent to the output section through the mode select decoder U13. It also reloads the BCD switch setting into the counters on the fly providing a continuous output equal to the counter input frequency divided exactly by the BCD switch setting. U13 is an eight to one multiplexer, with only three inputs used, controlled by a three bit binary code. In the

divide mode the DIV/DLY/BURST front panel switch (S1 on the schematic) sends a "zero" to U13 pin 11, the S0 input, and a "one" to pin 10 the, S1 input. The S2 input is grounded and permanently held to a "zero". This forms the binary 010 code (decimal 2) which enables the I2 input at pin 2. The inverted counter load pulse is connected here and passed on to the output section. The counter clock is enabled continuously as the low on S0 also forces a high at the output of nand gate, U9, at pin 8 and a low at the output of invertor U20 at pin 6. This low enables both the 25 MHz internal oscillator, U16, and the divide by 10 scaler, U2, which now provide a continuous clock. The counter load pulse then produces the divided down output frequency desired.

In the delay mode the terminal count is decoded at the output of U9 pin 8 as the DIV/DLY/BURST switch now places a high level on pin 13 of U9 and the S0 input of U13. This high is also sent to the clear input of flip flop U17 at pin 1 allowing it to be set any time the counter is running. This places a low on pin 1 of the four input gate U9 inhibiting it from generating a reload pulse at the terminal count. The terminal count is decoded at U9 pin 8, which goes low. This low is inverted by U20 to be a high at pin 6 and inhibits both the internal oscillator U16 and the external clock scaler U2. This holds the six decade counter at the terminal count. This high is also sent to the output section through U13, the multiplexer, to become the delayed output. This

is now a stable condition with the six decade counter stopped that exists until an external burst input pulse or a manual burst input is received. A positive burst input is inverted, passed through U15, used as an "or" gate, and clocks flip flop U17 at pin 3. This will cause the flip flop pin 6 to go high and place a high on gate U9 at pin 1. This enables the gate to decode the terminal count and reload the counters. This reload removes the terminal count, sets flip flop U17, enables all clocks, and starts the cycle over again. The manual burst input is controlled by switch, S1, and the de-bounce flip flop made up from the gates of U15.

In the burst mode operation is the same as the delay mode except that the inverted counter clock is gated to the output through the multiplexer, U13. The DIV/DLY/BURST switch in the burst mode position places a high on the U13 S0 input and a low on the S1 input. Since the S2 input is connected to ground, this places the binary 100 or decimal 1 address on the lines. This gates the inverted clock connected to the I1, pin 3, input to the output section. This allows the output to be the counter clock while the counter is running which produces the clock burst desired.

The output signal from the multiplexer, U13, at pin 5 enters the output section where it drives the three pulse forming circuits that generate the ADV OUT, OUT 1, and the OUT 2 outputs. While this signal is low it sets the U17 flip flop causing a high on the

Q output as pin 9 this enables the first nand gate, U23, at pin 2. The second gate, which drives the output, is connected as an invertor as both inputs are connected together. When this signal goes high it is coupled through the two nand gates in U23 and appears as the ADV OUT Pulse. This signal is also connected to the flip flop clock, pin, 11 through R37, a 2K resistor. The 51 PF capacitor, C36, connected form this clock input to ground causes a delay before the high level can toggle the flip flop. It takes the capacitor about 50 nsec to charge up to the clock threshold level. At the end of this delay the flip flop toggles, and its Q output goes low. This inhibits the first nand gate forcing its output high which is inverted by the second nand gate causing the ADV OUT level to go low forming a 50 nsec high level output. Diode CR1 and resistor R36 form a quick discharge path for C36. This is necessary, as the pulse width will be shorter if C36 is not discharged completely before the next pulse occurs. This circuit will follow the demultiplexer output for rep rates that are to fast to allow the flip flop to toggle.

The OUT 1 and OUT 2 signals are formed by programmable delays controlled by six bit binary code inputs. These binary inputs are generated from the front panel decade switches through proms U10 and U19 coded to produce a decimal to binary conversion. Pull up resistors on BCD switches S8 and S9 provide the input delay setting to the BCD to binary converter U10. U10 provides the

conversion necessary for the timer delay generator, U21. S12 and S13 provide the input delay setting to the BCD to binary converter U19. U19 provides the conversion necessary for the timer delay generator, U12. These are precision delay generators that can produce addressable timing delays of 1 through 99 nsec in 1 nsec increments. The output of U12 goes through the invertor, U20, then through the driver, U23 to OUT 1 at J5. The pulse width is controlled by delaying the reset pulse to the timer delay generator. Once triggered the output of the timer delay will go high after the set delay and stay high until it is reset. The reset line is connected to the output through resistor R10. The 51 PF capacitor, C37, connected form this reset input to ground causes a delay before the high level at the output can cause a reset. It takes the capacitor about 50 nsec to charge up to the reset level. At the end of this delay the output of the timer delay goes low removing the high at the output. R14 is a delay calibration range adjustment for the timer delay, U12, and is normally adjusted for a 99 nsec delay when the front panel delay setting is set to 99 nsec.

The 0 to 99 nsec delay for the OUT 2 pulse is generate the same way as that for the OUT 1 above except that the U21 timing delay is used. R15 is a delay calibration range adjustment for this. The 100 to 900 nsec delay is an additional function which also affects the pulse width delay circuit. The output of the timer

delay, U21 is connected to nand gate U1 at pin 9 and to the precision delay generator input, U26 at pin 1. It is also connected to the I0 input of the 8 to 1 multiplexer U26. U22 and U26 form a 10 to 1 multiplexer. If the output has been low for some time all outputs from the precision delay will be low, and the output of the multiplexer will be low. This signal is connected to the other input of the nand gate, U1 at pin 10. Since it is initially low it will force the output of nand gate U1 high at pin 28 and inhibit the high level output from the timer delay from getting through. This keeps the OUT 2 output low. The high level from the timer delay does go to the precision delay, U25, and to the multiplexer I0 input. The precision delay will produce outputs along its delay line at 100 nsec intervals. These are sequentially connected to the multiplexer such that the binary code of 0000 through 1001 (decimal 0 through 9) generated by the most significant digit of the front panel delay switches will select delay outputs of 0 through 900 nsec. Note that the 0 nsec connected to I0 of U26 is just the timer delay output. The two multiplexers can be connected in parallel as shown, as they are tri-state devices. The enable line is the most significant bit of the delay select code from the switch.

When the selected delay time is passed through to the output, the output of the multiplexer goes high. This opens the nand gate, U1 allowing its output to go low. This output is inverted by the

output driver nand gate and becomes the delayed OUT 2 output. The high from the multiplexer is connected to the timer delay reset through R21 and C38 to produce the desired pulse width as described for OUT 1 above.

MODEL HVP-5I-DIFF PULSER

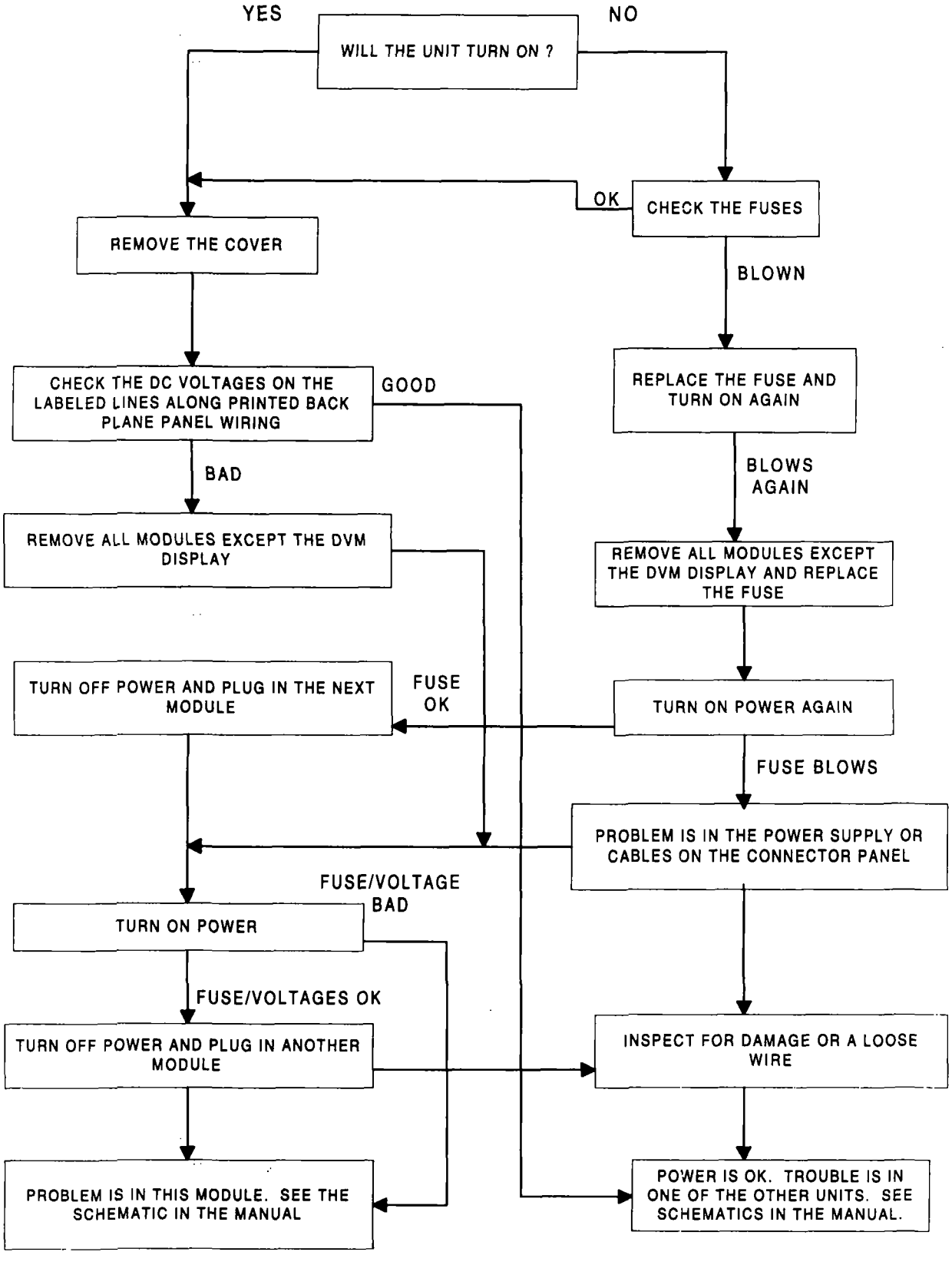
GENERAL:

The HVP-5I-DIFF pulser is a dual high voltage fast rise time pulser. It accepts a high voltage DC input and produces a pulse that goes from the high voltage level to ground on the output that receives a trigger. A differential pulse up to 8000 Vp 20 nsec in width can be generated by sending a trigger to each input phased 20 nsec apart. Pulse rates are limited by the capacity of the high voltage power supply and load capacitance with frequencies up to 5000 PPS being typical. Higher frequency units and units with inverted outputs are available by special order.

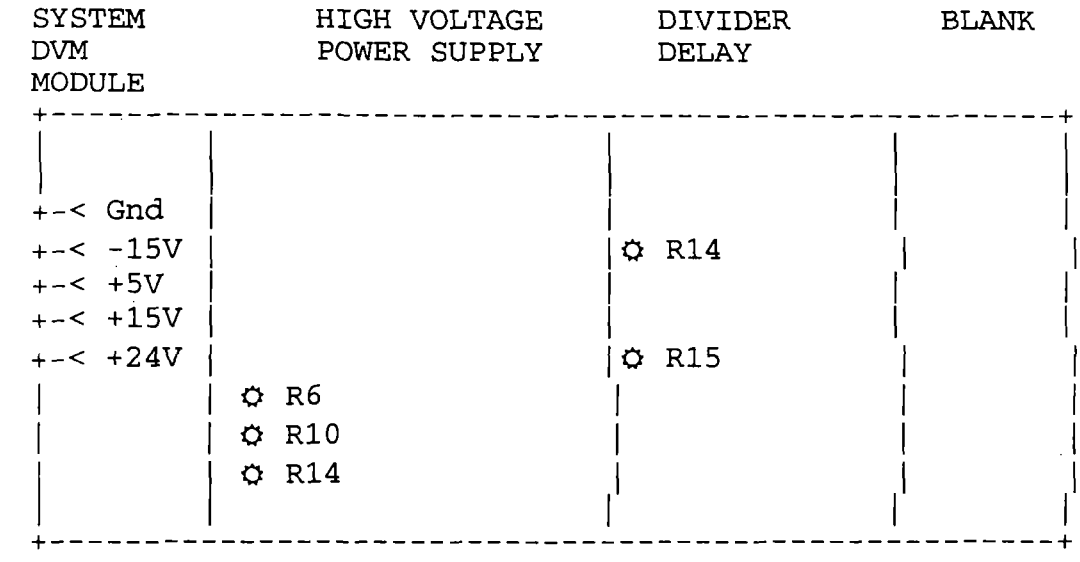
TROUBLESHOOTING FLOW CHART

WARNING UNAUTHORIZED REPAIR MAY VOID THE WARRANTY

Follow the flow chart below to isolate a failure to the plug in module level. The drawing shows the internal adjustments and test points available when the top cover is removed.



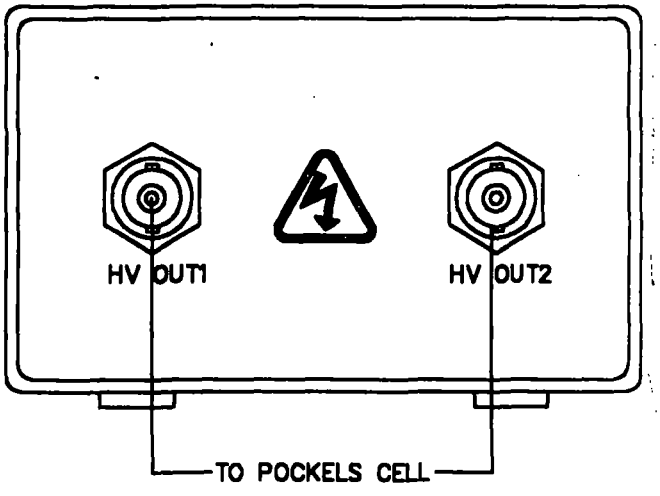
SYSTEM TOP VIEW WITH COVER OFF



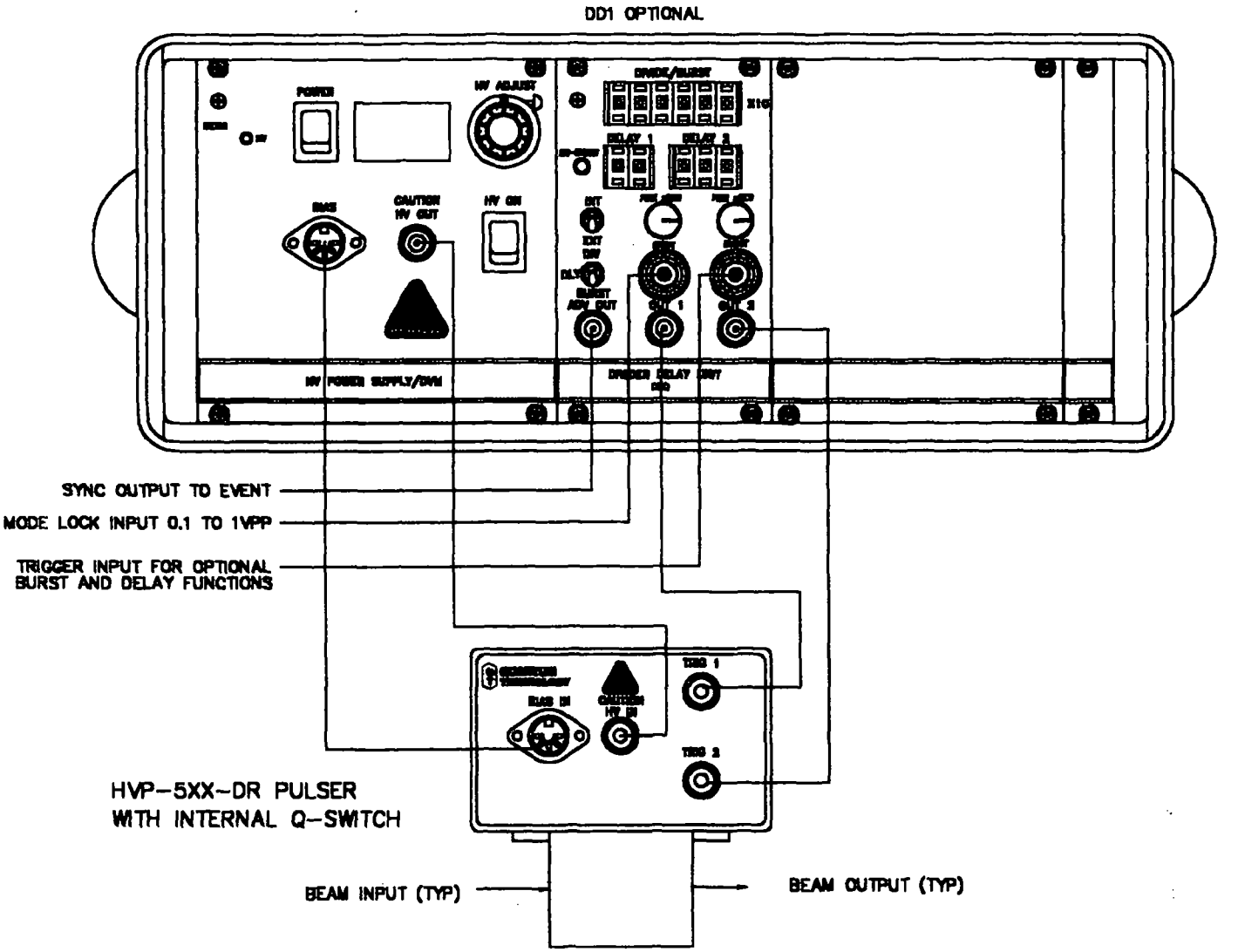
	ADJUSTMENT LOCATION	FUNCTION
*	R6 HV SUPPLY	LOW LIMIT ADJ
	R10 HV SUPPLY	METER CAL
**	R14 HV SUPPLY	HIGH VOLTAGE LIMIT
	R15 DIVIDER DELAY	DELAY 2 CAL
	R14 DIVIDER DELAY	DELAY 1 CAL

* High voltage limit for HVPS-9003

** Low voltage limit for HVPS-9003



REAR
HVP-590D-R
(SHOWING OPTIONAL MHV CONNECTORS)



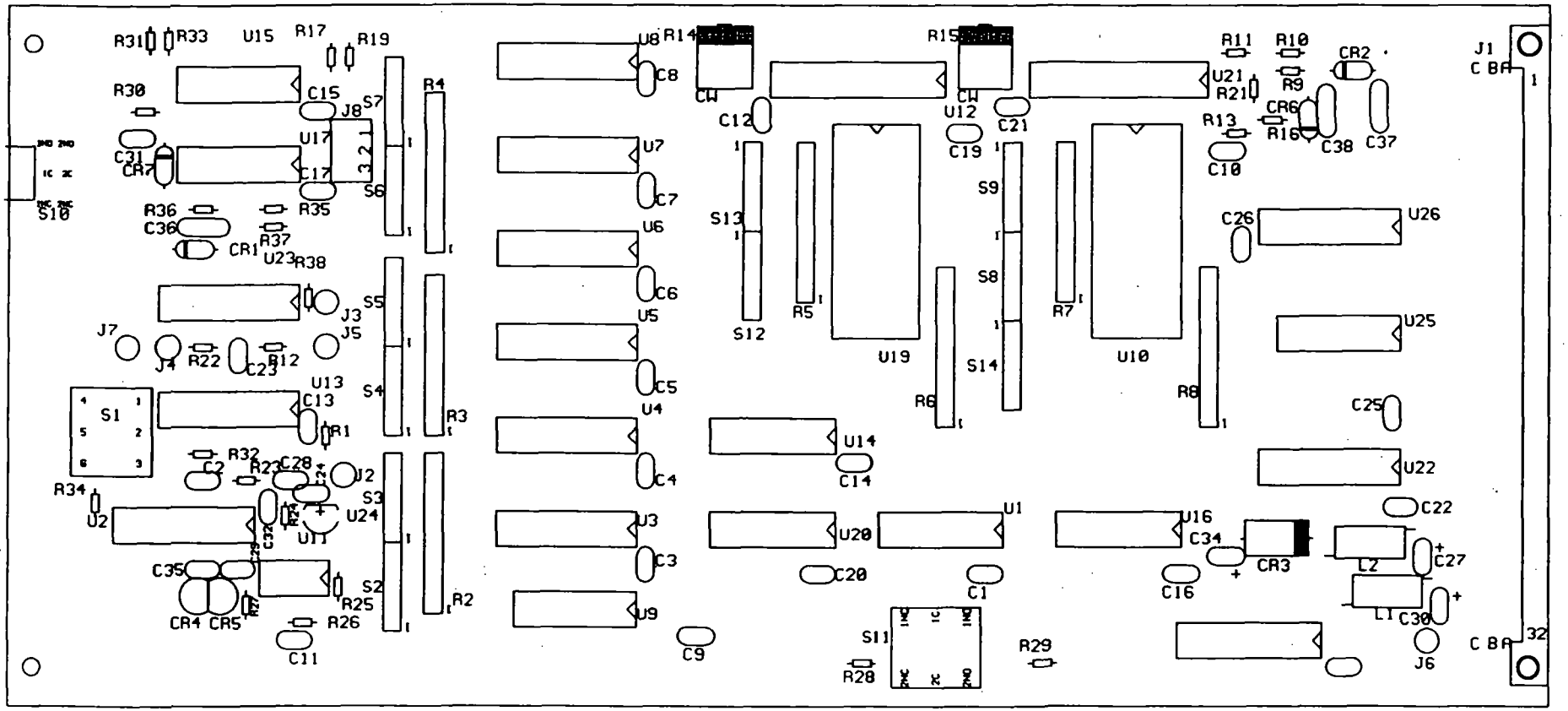
HVP-5I-DIFF DRIVER WITH Q-SWITCH

CABLE INTERCONNECTION

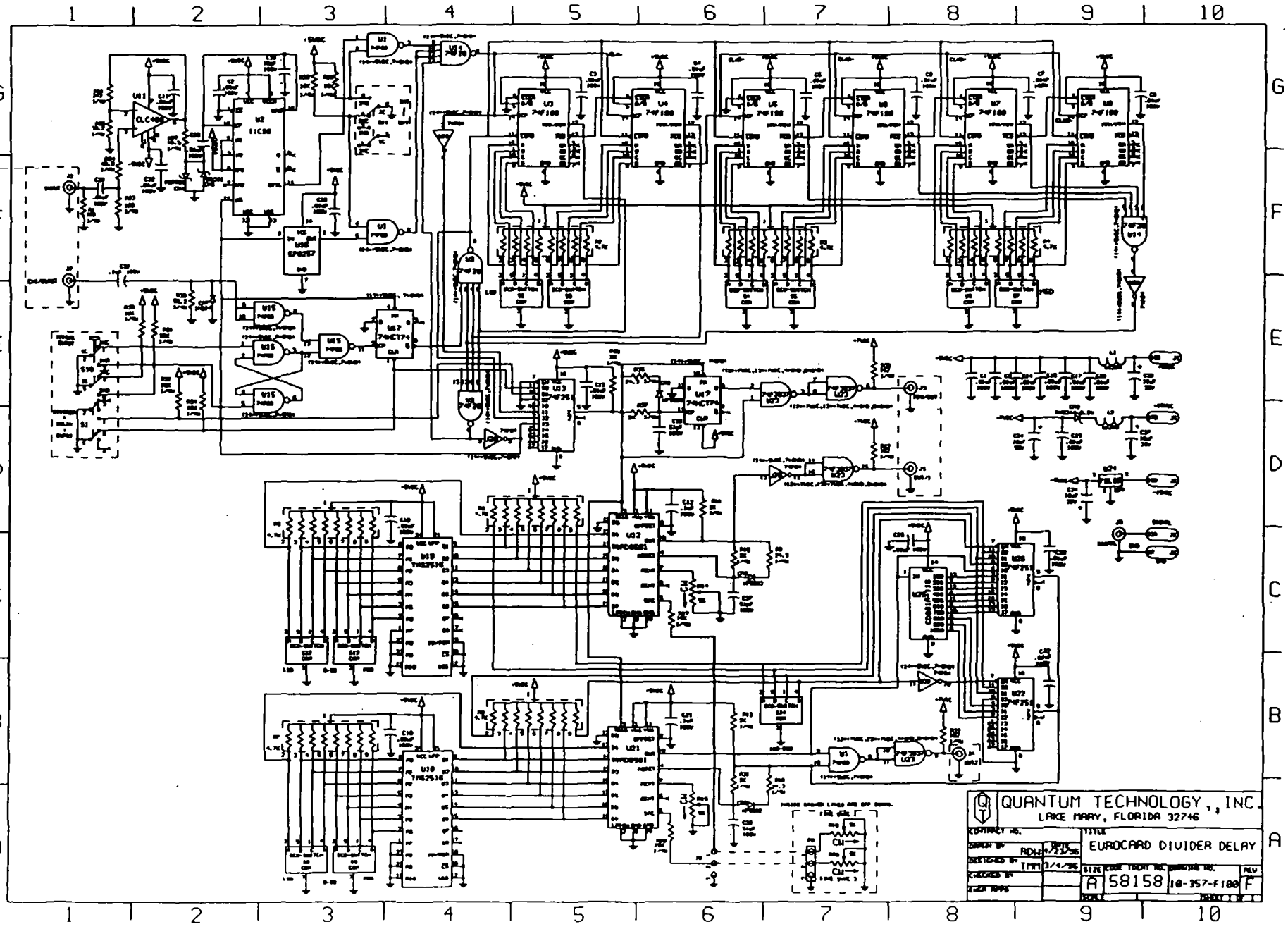
HVP5IDIFF

04/11/02
\lit\hvp51diff.dwg

SILKSCREEN



QUANTUM TECHNOLOGY, INC.		DESIGNED BY TMM	DATE 3/22/96
LAKE MARY, FLORIDA PHONE: (407)333-9348		PCB DESIGN RDW	DATE 4/23/96
		CHECKED BY	DATE
DRAWING NO. 10-357-E400	REV E	NAME EUROCARD DIVIDER DELAY	ENGR APPD / DATE


QUANTUM TECHNOLOGY, INC.
LAKE MARY, FLORIDA 32746
TITLE
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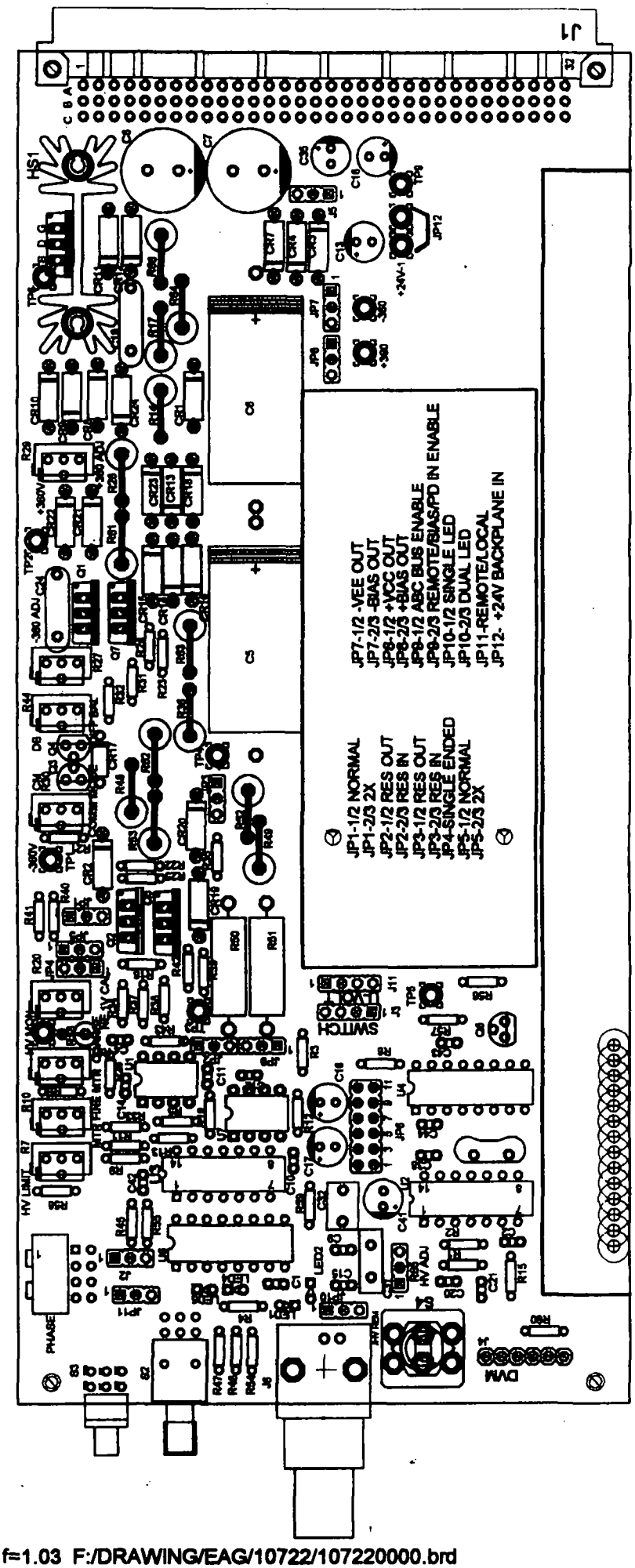

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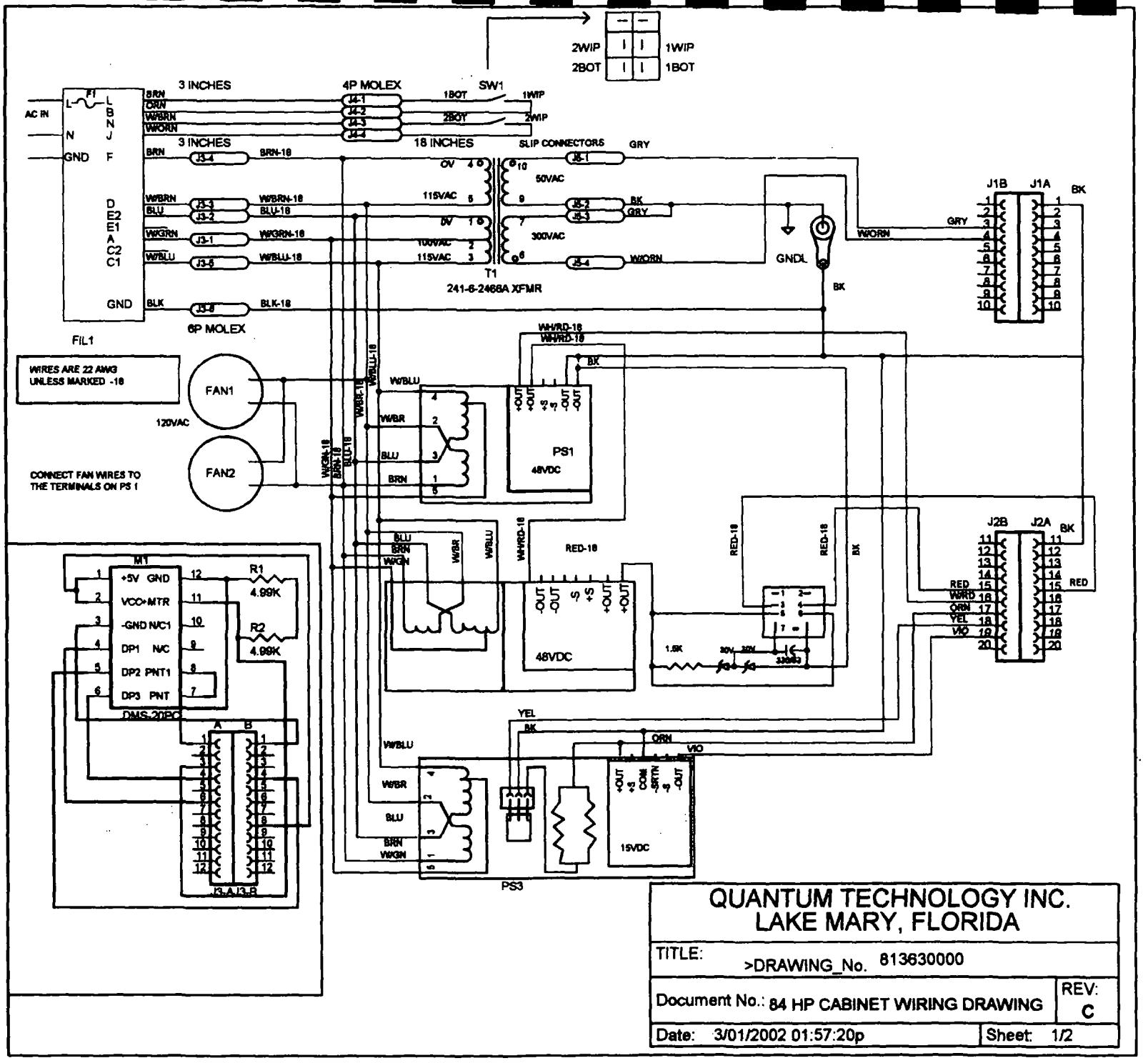
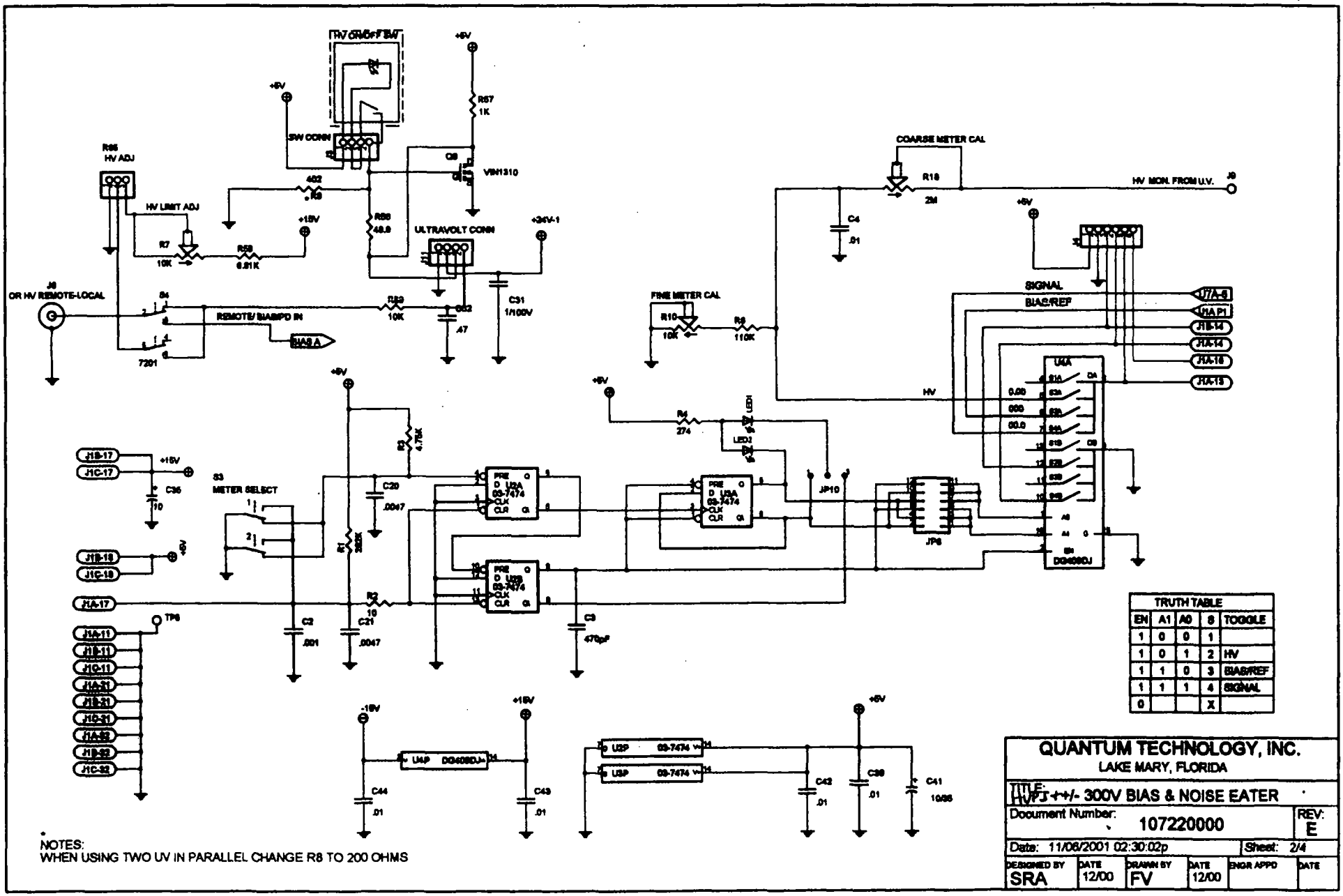




TRUTH TABLE				
EN	A1	A0	S	TOGGLE
1	0	0	1	
1	0	1	2	HV
1	1	0	3	BIAS/REF
1	1	1	4	SIGNAL
0			X	

NOTES:
WHEN USING TWO UV IN PARALLEL CHANGE R8 TO 200 OHMS

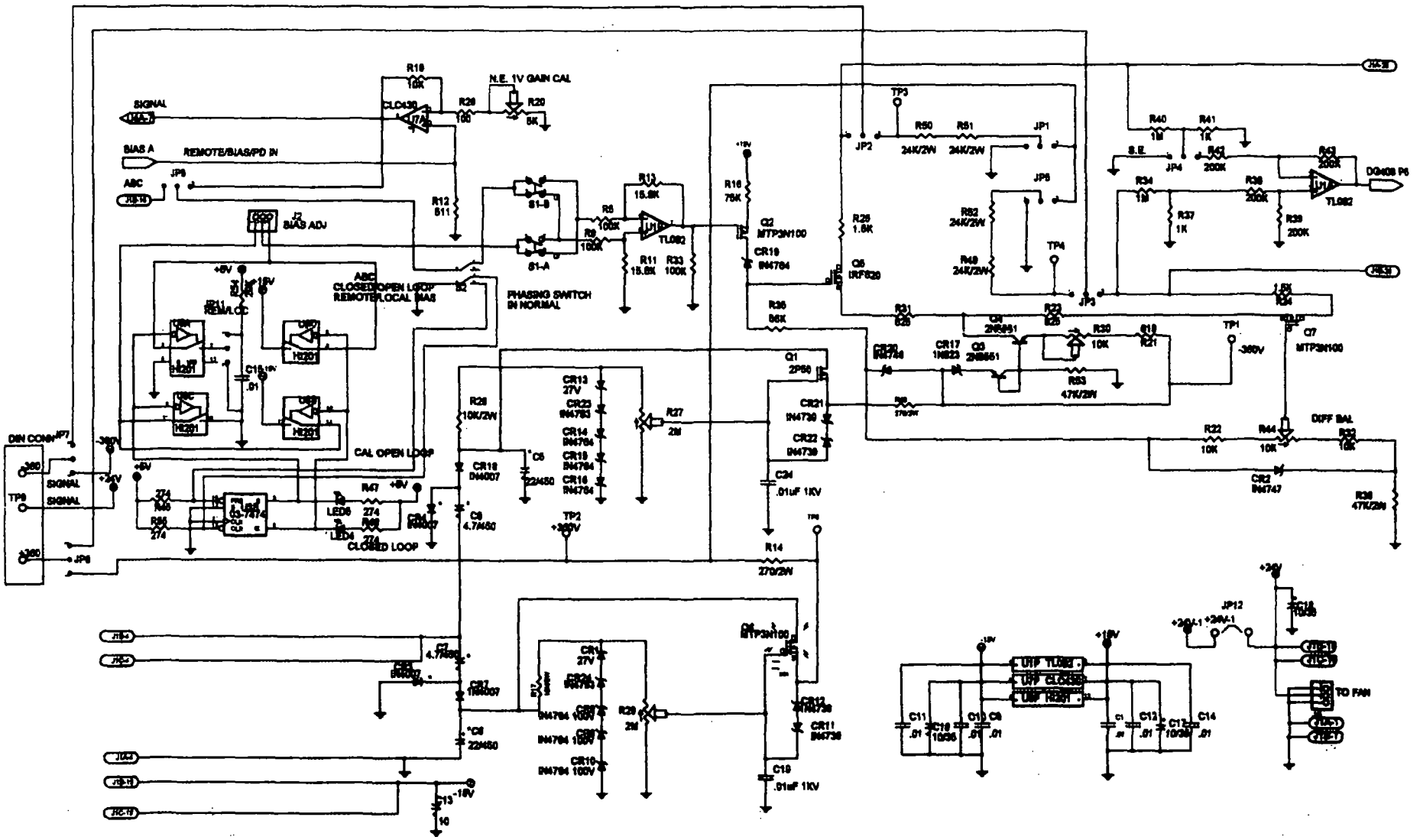
QUANTUM TECHNOLOGY, INC.
LAKE MARY, FLORIDA

TITLE: HVPJ +/- 300V BIAS & NOISE EATER

Document Number: 107220000 REV: E

Date: 11/06/2001 02:30:02p Sheet: 2/4

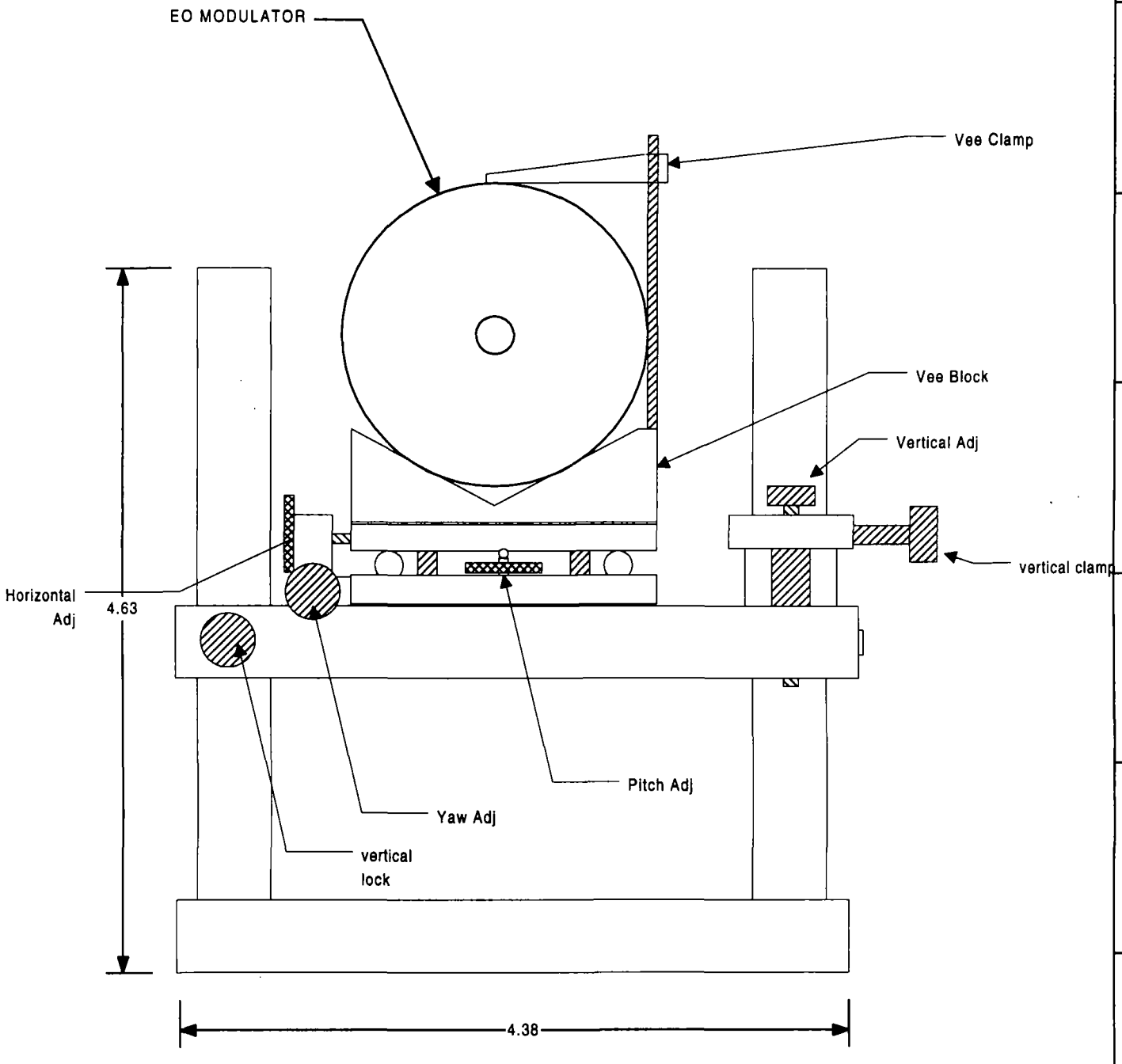
DESIGNED BY	DATE	DRAWN BY	DATE	ENGR APPD	DATE
SRA	12/00	FV	12/00		



JP1-2/3 NORMAL
JP2-1/2 RES ENABLE
JP3-2/3 RES ENABLE
JP4 S.E.
JP5-1/2 NORMAL
JP6-2/3 ZI
JP7-1/2 -VEE
JP7-2/3 -BIAS
JP8-1/2 +VCC
JP8-2/3 +BIAS
JP9-1/2 ABC BUS ENABLE
JP9-2/3 REMOTE/BIAS/PD IN ENABLE
JP10-1/2 SINGLE LED
JP10-2/3 DUAL LED
JP11-REMOTE/LOCAL

* NOTES.
1. NORMAL LEVEL: HV JMP C7, C8 OMIT CR3, CR4.
DOUBLE LEVEL HV: ABOVE INSTALLED, C8, C66 CHANGE TO 400VDC
2. JP13- INSTALL FOR 30 WATT HV SUPPLIES

QUANTUM TECHNOLOGY, INC. LAKE MARY, FLORIDA					
TITLE: +/- 300V BIAS & NOISE EATER					
Document Number: 107220000					REV E
Date: 11/09/2001 02:30:02p				Sheet: 1/4	
DESIGNED BY SRA	DATE 12/00	DRAWN BY FV	DATE 12/00	ENGR APPR	DATE



MODEL: MTM MOUNT WITH EOM			
SIZE A	FSCM NO	DWG NO N/A	REV =
SCALE 1 : 1		SHEET 1 OF 1	

MAIN CABINET POWER SUPPLY TEST DATA

Work Order No: E02-159 DATE: 8/26/02

Customer: Univ. of CA S/N: E02-159

Shipped Line Voltage: _____VAC

ELECTRICAL TEST:
MODEL PSM POWER SUPPLY/METER:

M CABINET (63 HP)_____ SWITCHER _____ LINEAR
L CABINET (84 HP)_√_ STANDARD LINEAR
XL CABINET _____ STANDARD LINEAR

Fusing: 100 VAC _____A Slo Blo 117 VAC _5_A Slo Blo
220 VAC _____A Slo Blo 250 vAC _____A Slo Blo

Tested line voltage
VOLTS AT: 100 VAC ____ 117VAC _√_ 220VAC _____ 240VAC ____

+20 to +28 V Supply:	N/A	VDC		VDC
+ 15 V Supply:	15.1	VDC		VDC
+ 5 V Supply:	5.02	VDC		VDC
- 15 V Supply:	-15.04	VDC		VDC
Other DC Supplies:	24.03	VDC	12.5 A	
		VDC	A	
50 VAC Supply:	63	VAC		VAC
350 VAC Supply:	372	VAC		VAC
T2-4, T2-5 117VAC fan	117.5	VAC		VAC
T2-1, T2-2 100VAC	104	VAC		VAC
T2-1, T2-3 117VAC	117.5	VAC		VAC
For 220V T2-3, T2-4		VAC		VAC

Meter cal 1500mv: OK DVM Reading

Decimal point: DP1 _√_ .000
DP2 _√_ 0.00
DP3 _√_ 00.0

Comments:

Checked By:

DATA SHEET HIGH HVP-5XX-D-R PULSER MODULE

Date: 8/26/02 Work order: E02-159

Ser No. E02-159D customer: Univ. of CA

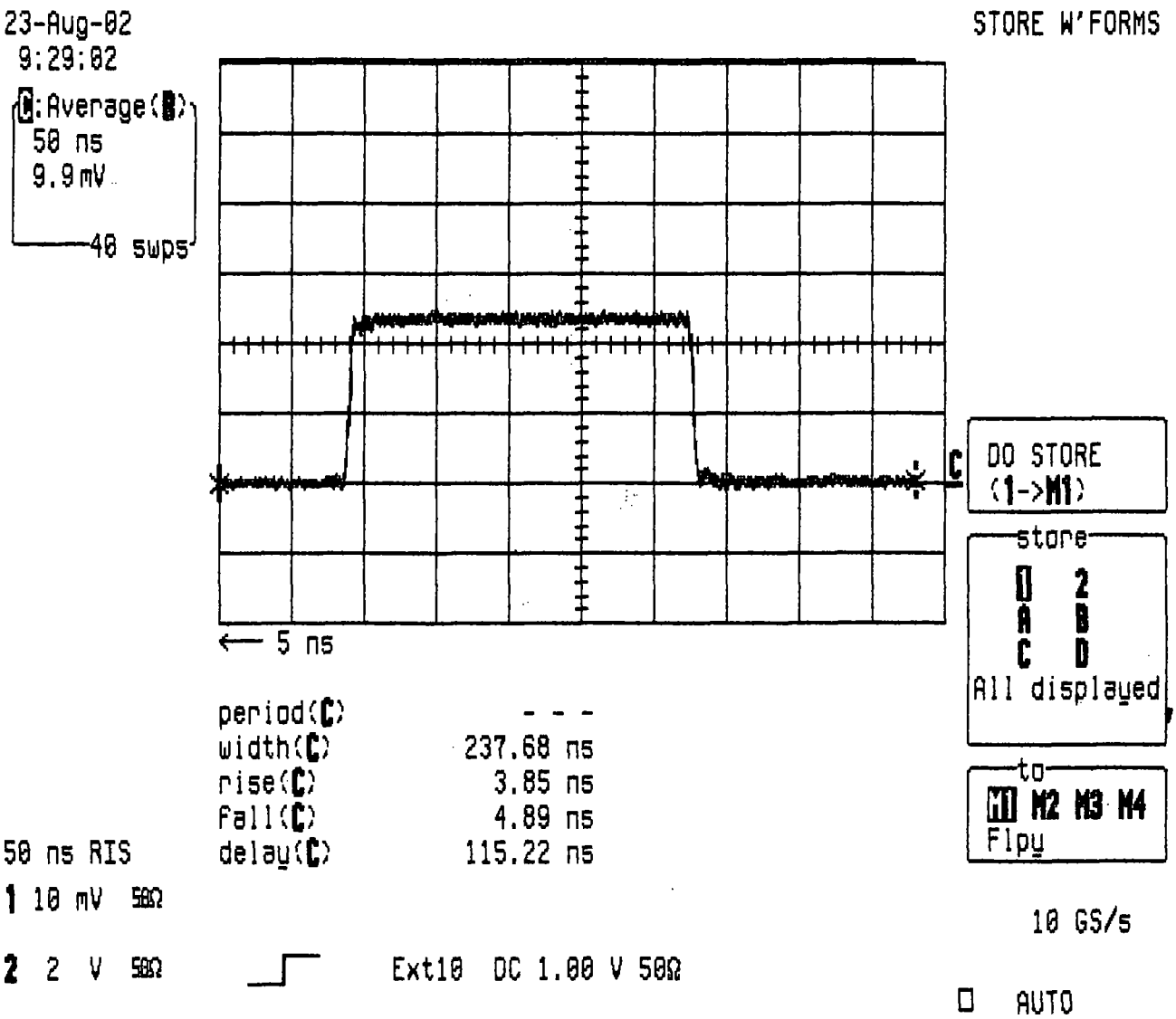
Model no: HVP-525D-R-50K

PARAGRAPH	TEST	RESULT
1.	LEADING EDGE RISE TIME	5 NSEC
2.	TRAILING EDGE FALL TIME	5 NSEC
3.	MINIMUM PULSE WIDTH TYPICAL	10 NSEC
4.	MAX Vpp OUT AT 5.1 KV IN	5.1 KV MAX
5.	MAX PULSE RATE CONTINUOUS	50 KHZ
6.	With cables	1 ft Length or N/A
7.	Mini DIN Bias	OK
	RG-59	
	RG-62LC (Low capacitance)	√
	TLC (Test Lead)	

NOTES: Shipped with QS-3-2.

SIGNATURE: 

F:\COMMON\WP51\1testdat\hvp5xxdr.dat Rev 8/26/02 11:40am



Detected Optical Response
SN:E02-159D

DATA SHEET 40SE-HVPS HIGH VOLTAGE POWER SUPPLY

Date: 8/26/02 Work order: E02-159

Ser No. E02-159A Customer: Univ. of CA

Model Number _____ HVPS-3006 3KV, 6.6 ma

Model Number _____ HVPS-6005 5KV, 5 ma

Model Number _____ HVPS-5006 6KV, 6 ma

Model Number _____ HVPS-9003 9KV, 3 ma

Model Number _____ HVPS-1060 1KV, 60 ma

Model Number _____ HVPS-6010 5KV, 12 ma

Model Number _____ HVPS-5060 5KV, 60 ma

Model Number √ HVPS-6040 6KV, 40 ma

Model Number _____ HVPS-9012 9KV, 12 ma

Model Number _____ HVPS-5001 5KV, 1 ma

Model Number _____ HVPS-9006 9KV, 6 ma

TEST DATA:

Meter calibration & DPX.XX √ OK

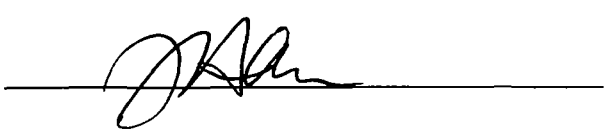
HV limit dial at 10 if provided 5.1 KV

HV disable check √ OK

Bias voltage 320 VDC

REMOTE/LOCAL option N/A OK VDC MAX= KV

Slow ramp up option _____ Yes √ No

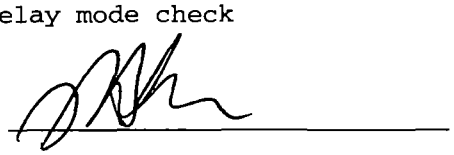
Test By: 

DATA SHEET DIVIDER/DELAY MODEL DD1-D

Date: 8/26/02 Work order: E02-159

Ser No.: E02-159B Customer: Univ. of CA

PARAGRAPH	TEST	PASSED/VALUE	
3.1	Divide by 10 scaling ADV OUT	50	NS
3.2	Delay 2, OUT 2 pulse width	65	NS
3.2	Delay 2, 10 to 90 NSEC steps	OK	
3.3	Delay 2, 1 to 9 NSEC steps	OK	
3.3	Delay 2, 1 to 25 NSEC vernier	25	NS
3.4	OUT 2 900 NS delay	900	NS
3.5	Max frequency 0 NSEC delay	470	MHZ
3.6	Delay 1, OUT 2 pulse width	50	NS
3.6	Delay 1, 10 to 90 NSEC steps	OK	
3.6	Delay 1, 1 to 9 NSEC steps	OK	
3.6	Delay 1, 1 to 25 NSEC vernier	34	NS
3.7	Burst mode external	OK	
3.7	Burst mode external 3 pulse groups	10	MHZ
3.7	Burst mode external max frequency	440	MHZ
3.8	Burst mode manual	OK	
3.9	Divider count accuracy	OK	
3.10	Sensitivity 50 MHZ input	35	MVpp
3.11	Divider max frequency	450	MHZ
3.12	Internal clock frequency	25	MHZ
3.13	Internal clock delay burst	OK	
3.14	Input to ADV OUT delay	111	NS
3.14	ADV OUT to OUT 2 delay	65	NS
3.14	Divide count delay	OK	
3.15	Delay mode check	OK	

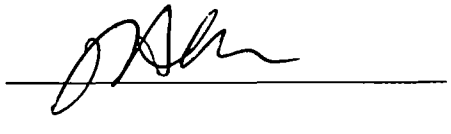
Signature 

DATA SHEET DIVIDER/DELAY MODEL DD1-D

Date: 8/26/02 Work order: E02-159

Ser No.: E02-159C Customer: Univ. of CA

PARAGRAPH	TEST	PASSED/VALUE	
3.1	Divide by 10 scaling ADV OUT	50	NS
3.2	Delay 2, OUT 2 pulse width	60	NS
3.2	Delay 2, 10 to 90 NSEC steps	OK	
3.3	Delay 2, 1 to 9 NSEC steps	OK	
3.3	Delay 2, 1 to 25 NSEC vernier	28	NS
3.4	OUT 2 900 NS delay	900	NS
3.5	Max frequency 0 NSEC delay	440	MHZ
3.6	Delay 1, OUT 2 pulse width	50	NS
3.6	Delay 1, 10 to 90 NSEC steps	OK	
3.6	Delay 1, 1 to 9 NSEC steps	OK	
3.6	Delay 1, 1 to 25 NSEC vernier	30	NS
3.7	Burst mode external	OK	
3.7	Burst mode external 3 pulse groups	10	MHZ
3.7	Burst mode external max frequency	430	MHZ
3.8	Burst mode manual	OK	
3.9	Divider count accuracy	OK	
3.10	Sensitivity 50 MHZ input	35	MVpp
3.11	Divider max frequency	440	MHZ
3.12	Internal clock frequency	24.9	MHZ
3.13	Internal clock delay burst	OK	
3.14	Input to ADV OUT delay	110	NS
3.14	ADV OUT to OUT 2 delay	55	NS
3.14	Divide count delay	OK	
3.15	Delay mode check	OK	

Signature 

QS SERIES POCKELS CELLS INTRUCTION MANUAL

1.0 SCOPE

This is an instruction manual for the installation and alignment of Quantum Technology's QS Series Pockels Cells, whether used in shuttering applications such as pulse slicing and extraction or for Q-switching.

1.1 INTROCUTION

The Pockels Cell Q-switch can produce laser pulses of short duration (typically 6-50nsecs depending upon system configuration) and high peak power by storing energy in the laser rod for the first half of the flashtube pulse and then releasing it. This is achieved by applying a high voltage across the crystal in the Pockels cell. This voltage causes rotation of the polarization of the laser beam, which then goes through a polarizing filter. The effect is a change in intensity of the beam. The Pockels cell, in conjunction with the polarizing filter, thereby acts as an electro-optic shutter and inhabits lasing. Removal of this high voltage, after a period set to maximize the stored laser energy, results in the Q-switched laser pulse.

In pulse slicing or extraction of pulses from a mode-locked pulse train, the Pockels cell is placed external to the laser (between two crossed polarizers). A fast high voltage pulse will result in selection of the laser pulse that is coincident with the high voltage. Widening the high voltage pulse would result in the selection of more than one pulse if so desired.

1.2 GENERAL CHARACTERISTICS

The Pockels cell is a sealed unit with anti-reflection coated windows at each end centered with the crystal faces to minimize disturbance of the beam path. The void between the window and the crystals is filled with dry nitrogen so that there is no moisture to effect polish of the crystal faces, since BBO is hygroscopic. The Pockels cell is hermetically sealed to make it leak-proof. The largest of the QS series Pockels cells, Model QS-6-2, has a 6mm aperture requiring two BBO Crystals to keep V¼ to a reasonable level, single V¼ is inversely proportional to crystal length and directly proportional to wave-length and crystal thickness.

This device is to be used only as an intra-cavity Q-Switch. The HW version is water cooled so as to handle up to 150 watts.

All Quantum's Pockels cell utilize high quality, strain-free crystals. The crystals of the QS series are plated with transverse electrodes for uniform electric fields and resistivity is greater than 10^{10} ohm-cm.

1.3 CAUTIONARY NOTE

APPLICATION OF A CONTINOUS DC VOLTAGE TO THIS POCKELS CELL COULD RESULT IN ITS PREMATURE FAILURE.

The following parameters are the maximum allowable voltages for all Quantum Technology Pockels Cells:

POCKELS CELL SERIES	CRYSTAL MATERIAL	MAXIMUM VOLTAGE
QC	KD*P 10KV	Pulses W/Maximum 3%Duty Ratio No DC[1]
QS-3, QS-3-2	BBO	5.2KV AC or DC[2,3]
QS-4, QS-4-2	BBO	7.2KV AC or DC[2,3]
QS-6-2	BBO	7.2KV AC or DC[2,3]
LN	$LiNbO_3$	10KV AC or DC[2]

NOTE 1: AC Voltages in excess of 3% duty ratio (>1 sec.) or DC voltage may cause premature failure due to migration of electrode material into the crystal material, causing thermal runaway. It is suggested that a quarterwave plate be used between the Pockels cell and the rear laser mirror.

NOTE 2: AC Voltages in excess of 3% duty ratio (>1 sec.) or DC voltage may result in a temporary shift in optical transmission when placed between polarizing optics. This will be seen as a slow drift in transmission over a 1-10 minute interval and may be compensated for by re-adjusting the applied voltage. This effect is more pronounced in $LiNbO_3$ than in BBO Pockels cells.

NOTE 3: The maximum voltages for BBO Pockels cell is different for different apertures because the breakdown of the applied voltage occurs across the aperture.

POCKELS CELL/MODULATOR QUICK SET-UP

This alignment procedure consists of actually four sections. Section A is to be used when the Pockels cell and polarizer option is ordered. These will have been factory aligned and mounted together. Section B is the complete optical alignment for the Pockels cell and optional polarizer. You will need Vee block or optical mount capable of X, Y translation, pitch, yaw and rotation about the optical axis. Section C is the complete optical alignment for pulse picker or extra cavity applications when supplied without a polarizer. Section D is the optical alignment for intracavity Q-Switch applications.

SECTION A: Pockels Cell/Modulator with Polarizer First Time Alignment Instructions

1. Perform these instructions if the Pockels cell and polarizer were already prealigned by the factory and were not disturbed.

2. Hook up all the cables to modulator and accessories per the interconnection diagram supplied with the modulation system. If a system was not supplied, then attach the Pockels cell to driver or drive source to be used.

3. Insert the modulator into a suitable optical mount.

4. Rotate the modulator so the connectors are vertical. Critical adjustment will be done later.

5. Center the laser beam in the aperture of the modulator so the beam is exiting cleanly. Lower the laser power to less than 100mW.

6. Fix a white paper as a target about 1 meter down the optical path from the modulator. Place a pencil dot to show beam center on the paper.

7. Apply a piece of scotch invisible tape to the input end caps to diffuse the beam.

8. A bulls eye pattern will appear as shown in figure 3. This is the familiar "Maltese Cross" as observed in uniaxial birefringent crystals when illuminated in the optic axis (or Z axis) direction.

9. Using the pitch and yaw axis adjustments of the mount, align the cross pattern centered on the dot as show in figure 1.

10. Remove the diffusing tape and measure the optical transmission with a power meter.

11. Minimize the optical transmission by rotating the cell about the beam axis, trying not to disturb the modulators pitch or yaw adjustments.

12. Ensure that the cell is still aligned by repeating steps 7, 8 and 9.

13. The beam power should be very close to an optical minimum. Slight adjustments in pitch and yaw may further reduce the observed minimum. This will be best done by observing the minimum under dynamic conditions as observed on an oscilloscope using a high speed photo detector.

14. This completes this alignment procedure.

SECTION B: Pockels Cell and Polarizer Alignment Instructions

1. Perform these instructions if the Pockels cell and polarizer alingment was disturbed or needs to be realigned.

2. Remove the polarizer from the Pockels cell by loosening the set screw(s) that is attaching it to the cell.

3. Hook all the cables to the modulator and accessories per the interconnection diagram supplied with the modulation system. If a system was not supplied, then attach the Pockels cell to driver or driver source to be used.

4. Place the polarizer crossed to the input beam.

5. Insert the Pockels cell into a suitable optical mount before the polarizer.

6. Rotate the modulator so the connectors are vertical. Critical adjustment will be done later.

7. Center the laser beam in the aperture of the modulator Pockels cell so the beam is exiting cleanly. Lower the laser power to less than 100 mW.

8. Fix a white paper as target about 1 meter down the optical path from the modulator. Place a pencil dot to show beam center on the paper.

9. Apply a piece of scotch invisible tape to the input end caps to diffuse the beam.

10. A bulls eye pattern will appear as shown in figure 3e. This is the familiar "Maltese Cross" as observed in uniaxial birefringement crystals when illuminated in the optic axis (or Z axis direction).

11. Using the pitch and yaw axis on the mount align the cross pattern centered on the dot as shown in figure A1.

12. Apply a high voltage DC to the modulator by one of three ways:

    1. From the High Voltage DC power course output on the controller.

    2. By feeding a constant DC 5 volt level to the controller input to enable the HV driver to output on at DC.

    3. Use another external HV DC supply.

13. Measure the optical power through the modulator with a power meter.

14. Adjust the voltage going to cell so that a minimum transmission is obtained.

15. Maximize the transmission by adjusting the cell rotationally about the beam axis trying not to upset the modulators pitch or yaw adjustments.

16. Adjust the applied voltage to ensure that the transmission is at maximum.

17. Ensure that the cell is still aligned in pitch and yaw directions by repeating steps 7, 8 and 9 and setting the applied voltage to zero.

18. With the voltage off and the diffusion tape removed, the beam should be very close to an optical minimum. Slight adjustments in pitch and yaw may further reduce the observed minimum. This will be best done by observing the minimum under dynamic conditions as observed on an oscilloscope using a photo detector.

19. Measure the optical minimum.

20. Remove the polarizer from the optical mount and attach it to the modulator. Rotate the polarizer till the minimum in step 17 is attained.

21. Repeat step 16 to ensure the cell is aligned at a proper minimum.

22. This completes this alignment procedure.

SECTION C: The Pockels Cell/Modulator for Pulse Picker, Extra Cavity Applications.

These instructions are for Pockels cells or modulators as your particular case may be.

1. Hook up all the cables to modulator and accessories per the interconnection diagram supplied with the modulation system. If a system was not supplied, then attach the Pockels cell to driver or drive source to be used.

2. Insert the modulator into a suitable optical mount. A Vee block with pitch and yaw adjustments works best.

3. Rotate the modulator so the connectors are vertical. Critical adjustment will be done later.

4. Center the laser beam in the aperture of the modulator so the beam is exiting cleanly. Lower the laser power to less than 100 mW, (typically).

5. Fix a white paper as a target about 1 meter down the optical path from the modulator. Place a pencil dot to show beam center on the paper.

6. Apply a piece of scotch invisible tape to the input end caps to diffuse the beam.

7. A bulls eye pattern will appear as shown in figure 3. This is the familiar "Maltese Cross" as observed in uniaxial birefringent crystals when illuminated in the optic axis (or Z axis) direction.

8. Using the pitch and yaw axis adjustments of the mount, align the cross pattern centered on the dot as shown in figure 1.

9. Remove the diffusing tape and usually or by an optical power meter, fine tune modulator for the best optical minimum. Recheck steps 7, 8 and 9 to check if you are not significantly off the center of the cross.

10. If HV DC is available to be applied, then with the DC voltage (or HV pulse) applied observed the level on a power meter (or oscilloscope). If not then perform the observation with a HV pulse and oscilloscope.

11. Rotate the cell about the optical axis without changing the pitch or yaw axis. A Vee block with pitch yaw adjustments works best.

12. The total range of motion should not be more than +/- 5 degrees. Lock the cell rotation when the optimum rotation position is determined. It may be necessary to check steps 7, 8 and 9 again in case the pitch or yaw moved.

13. This completes this alignment procedure.

SECTION D: Pockels cell Alignment For Intracavity Q-Switch Applications.

1.4. PITCH/YAW ALIGNMENT

For proper operation of the Pockels Cell, the cell has to be positioned so that its optic axis is aligned to the beam to within 10 seconds of arc. Moreover, the X and Y axis of the crystal must be set parallel and perpendicular to the plane of polarization of the laser. The X and Y crystallographic axis of the crystal is horizontal when the high voltage connectors are horizontal. Parallelism between the crystal optic axis and the input laser beam is also important. This is achieved by mounting the Q-switch in an optical mount with three degrees of freedom along the X, Y and Z.

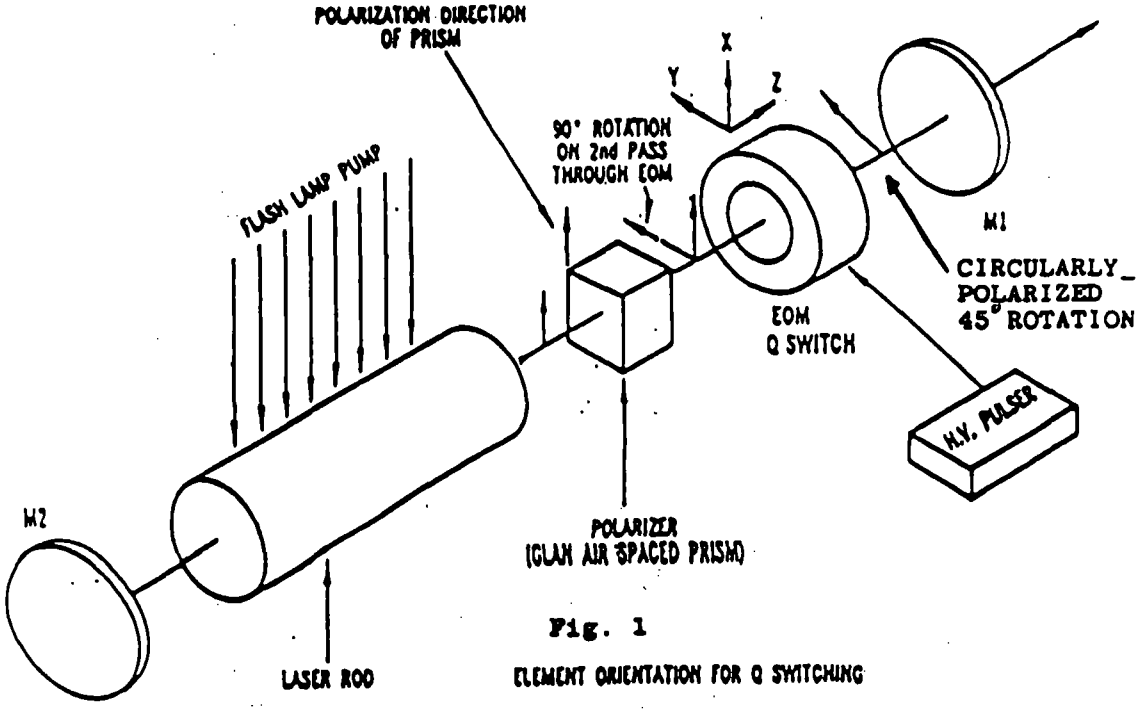
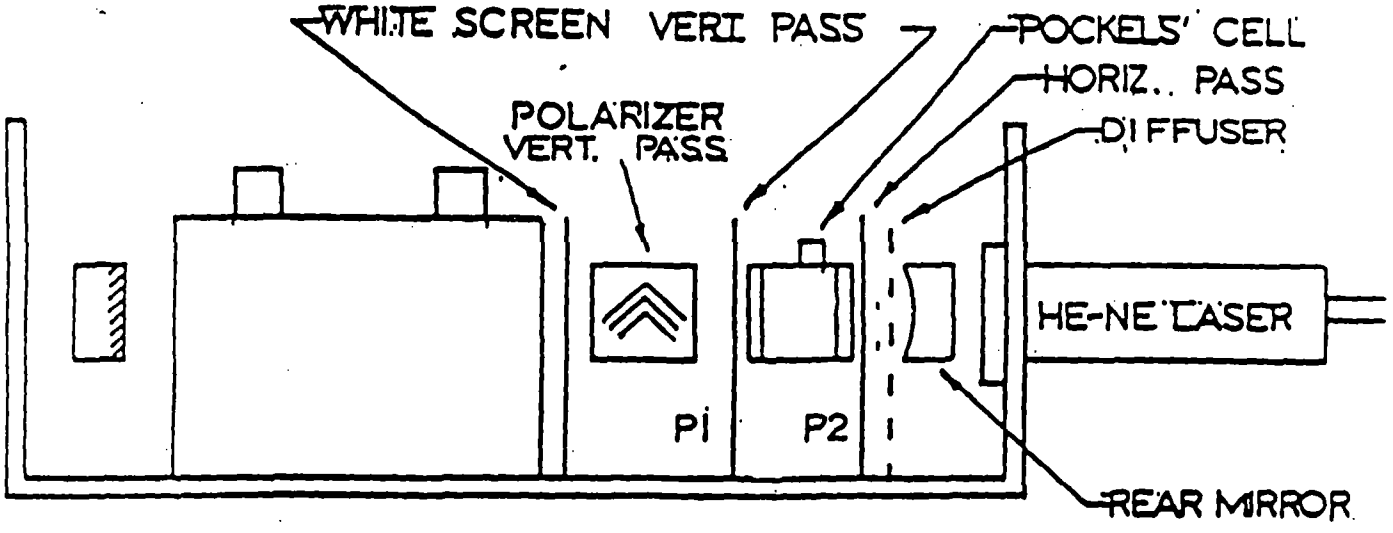


Fig. 1 ELEMENT ORIENTATION FOR Q SWITCHING

A typical arrangement of components is shown in Fig. 1. The inclusion of the polarizer is required if the laser rod output is not strongly polarized. Its presence, however, does improve system performance by raising the threshold for spontaneous emission.

1. Install the Pockels Cell so that the connector is aligned either parallel or perpendicular to the polarization plane of the laser.
2. Set up a HeNe alignment laser (Fig.2) so that it is collinear with the pulsed laser beam.
3. Place a gelatin polarizer P_1 (Polaroid sheet HN 32 or similar) between the Pockels Cell and the Q-switch prism polarizer so that polarizer P_1 and prism polarizer have their polarization planes parallel to each other.
4. Place another gelatin polarizer, P_2 crossed to this in contact with the other face of the Q-switch.
5. Place a diffuser between the HeNe laser and input polarizer P_2 crossed to this in contact with the other face of the Q-switch.
6. Place a diffuser between the HeNe beam projected onto the white screen.

A pattern consisting of a central black cross surrounded by concentric rings will appear on the screen. The optic axis is perfectly aligned when the bright central HeNe spot falls on the point of symmetry of the pattern as shown in Fig.3. It may be helpful to remove the Q-switch prism polarizer during this alignment. Also, it may be necessary to move the diffuser and the screen back and forth to obtain the clearest image on the screen. Which will appear brighter if the laboratory lights are switched off.



TYPICAL ARRANGEMENT FOR SETTING TILT OF POCKELS' CELL

Fig. 2

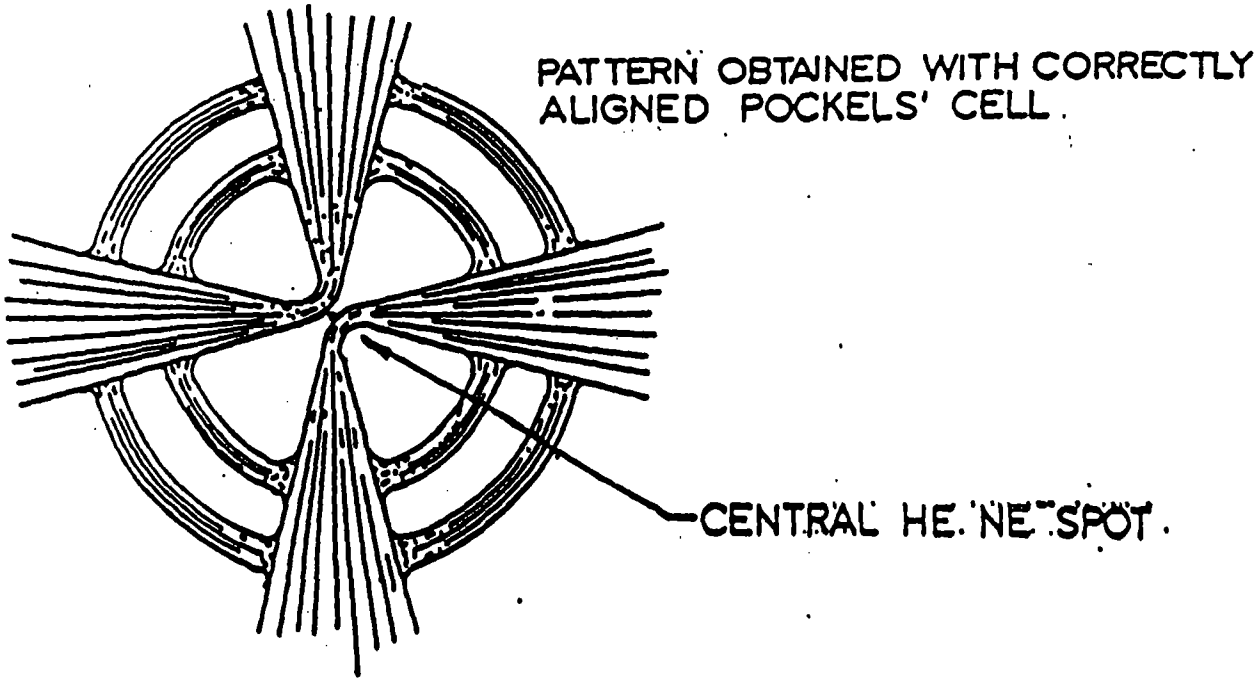


Fig. 3

1.5 ROTATIONAL POCKELS CELL ALIGNMENT

The following procedure should be followed for further improvement of the rotational alignment of the Pockels Cell.

1. Rotate the polarizer P_2 through 90° so that its polarization plane is parallel to that of P_1. The central pattern on the screen will now consist of four dark areas disposed about the center and at an angle of 45° to the vertical and horizontal (Fig. 4).
2. With the bias control set at a minimum, connect the Pockels Cell to the drive unit and switch on the unit. Gradually raise the bias voltage while observing the pattern projected on the screen.
3. Slowly rotate the Pockels Cell, which causes two of the dark areas in the projected pattern to move towards each other along the 45° axis (Fig. 4B). The Pockels Cell is correctly adjusted when they merge to form a diamond shape at the center.

If unattainable, set polarizer P_2 crossed to polarizer P_1 and repeats the procedure for Lateral Pockels Cell Alignment (para. 1.4).

Figure 5 is the pattern attained with the full voltage applied, resulting in maximum extinction.

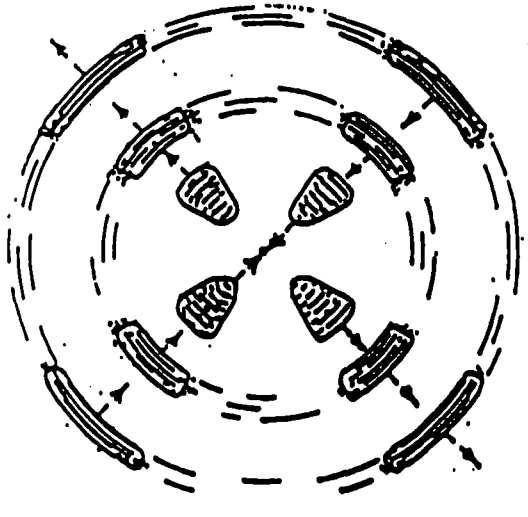


Fig. 4

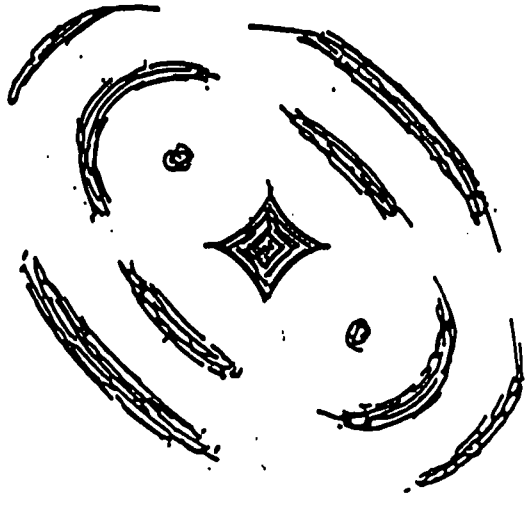


Fig.5

1.6 SWITCH NOTES:

1. On all pockels cells the damping method to hold the Pockels cell must be isolated from ground to withstand 10KV: metallic surfaces must not be in direct contact with the Pockels cell. If the pockels cell is to rest on a metallic surface. The plastic body and/or any fill screws must be installed from the base by .015" thick kapton sheet or equivalent.

1.7 WATER-COOLED CONNECTION

QS-Series Pockels Cells with a "W" suffix in its model number are water-cooled devices requiring a source of flowing water, at a rate of 1 - 2 liters per minute. This water should be de-ionized to prevent the build-up of scale, and, at the least, be filtered. Increase the water flow so that the water leaving he Pockels cell is close to room temperature with the Pockels cell operating at the desired power.

WARNING: COPPER TUBES MAY CARRY HV CHARGE UNDER PULSED HV OPERATION

The water should be de-ionized also, because under pulsed HV operation, the copper tubes may develop a HV charge. Faster risetime is observed if the copper tubes are not grounded, or not shorted by the use of non-de-ionized water. If it is necessary to ground the tubes, a pin socket on the curved end of the tubes may be used to connect to the ground lug on the driver rear case.

Connection to the Pockels cell is with ¼" inside diameter flexible tubing and a hose clamp. Right angle ¼" hose adapters are supplied to these brass connect to your flexible tubing. Please orient the direction of couplings before tightening them down as they "swage" down permanently on the copper tubing of the cell.

1.8 SINGLE CRYSTAL VERSIONS OF THE QS-6-2-HW

In these types of cells, the cells are provided as "matched" set. The single crystals within each cell are mounted close to the curved end of the water connectors on the cell. In so doing, the curved ends of the cells should face each other. As required, a quaterwave plate may be placed between the 2 cells. The + and - labels on the cells indicate that pairs, S/N ending in A and B, 2.

C and D should have the same wire connection to the driver. That is, the + of cells, A & B should go to the same driver outputs (either Out 1 or Out 2) for example and so on. If cell A and D need to operate with each other, then, it may be necessary to interchange the wires going to the +'s and -

's and determine the correct phasing for this new set, (the + of one may have to connect to the - of the other one for proper operation). For optical alignment the pitch and yaw of each cell will have to be adjusted independently.

1.9 WARRANTY

Please do not attempt to take the Pockels cell apart. In case of any problem, contact our Engineering staff. The Pockels cell is guaranteed for a period of three months from the date of invoice and may be returned to our Service Department within the warranty period. Please obtain prior authorization and proper shipping instructions before returning any device. We reserve the right to either repair, replace of refund any failed device, at our option.

For KD*P, or AD*P Pockels either QS or QB Series:

Operation of the Pockels cell by applying DC voltage or a duty cycle resulting in greater than 3% average AC voltage across the cell may cause premature failure and voids the warranty.

Quantum Technology reserves the right to make changes on details of the design and/or construction of any device, either before or after delivery, so as to ensure the highest quality of that device.

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POCKELS CELL TESTING

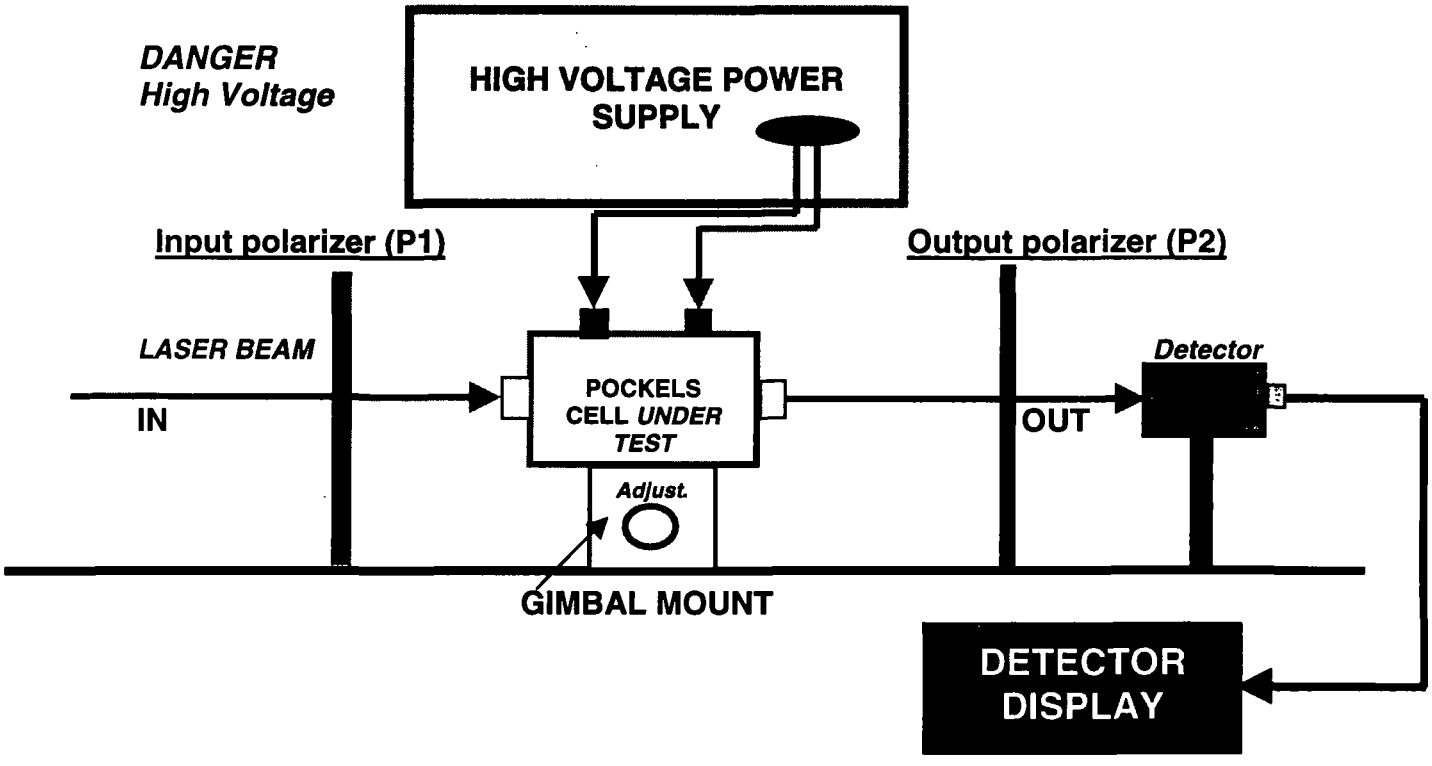
GENERAL

This manual contains general testing of Pockels cells produced by Quantum Technology. It is a useful guide for alignment within a system as well as, a QC aid for incoming inspection, and basic failure analysis.

APARATUS (recommended)

OPTICAL BENCH OR RAIL
TWO POLARIZERS (see text)
ONE TEST LASER - Preferred HeNe @ 633nm ~1mW CW
ONE DETECTOR for use within wavelength of test laser
ONE DISPLAY – for detector, either a meter or oscilloscope
ONE ROLL OF TRANSLUCENT TAPE – like Scotch invisible tape
ONE NEGATIVE LENS – Approximately -25mm
GIMBALL MOUNT TO ADJUST POCKELS CELL while under test
POCKELS CELL – *to be tested*
POCKELS CELL'S TEST DATA SHEET – *supplied with the Pockels cell*
WRITING MATERIAL
WHITE PIECE OF CARDBOARD OR PAPER
LASER POWER METER

When familiar with testing Pockels cells, more specialized testing may be setup for a particular application.



GENERAL SETUP FOR POCKELS CELL TESTING

Figure 1

INPUT/OUTPUT POLARIZERS – for this test they can be sheet polarizers if the test laser is in the visible range between 633nm (HeNe) and ~ 532nm. A CW power level of between 0.5mw~1mW is recommended. For reference, all tests in this procedure used 633nm-wavelength laser.

GIMBAL MOUNT – for YAW and PITCH adjustment of the Pockels cell. Rotational motion is not necessary, if the terminal are carefully placed in the "up" position as shown in the above drawing.

DETECTOR and DETECTOR DISPLAY – these devices are to be capable of indicating the intensity level of the source laser without saturating. A photodetector and oscilloscope or a low-level power meter can be used for this purpose.

HIGH VOLTAGE POWER SUPPLY – the range of this supply is up to 9KV depending of the Pockels cell under test. *This voltage is dangerous can be lethal.* Experienced personnel should only perform these tests. In some cases the Pockels cell driver can be used as the high voltage source, see the instruction manual for the particular unit used.

POCKELS CELL UNDER TEST – The Pockels cell under test can be one of the three basic models produced by Quantum Technology. The QC-series is KD*P, the QS-series is BBO, and the LN-series is lithium niobate. See table below for *approximate* halfwave voltages for 633nm. Consult the Pockels cell data sheet for the test voltage used for the particular cell.

QC- series (KD*P)	***QS- series (BBO)***	***LN – series (Lithium Niobate)***
~ 4 KV	**~ 8.1 KV**	**~ 1.4 KV**
Aperture: 6mm	*Aperture: 6mm*	*Aperture: 6mm*

VOLTAGE COMPARISON TABLE

NOTES:

1) **The larger the Pockels cell aperture – the greater the voltage**
2) **Dual crystal Pockels cells for QC and QS series require half the voltage shown in the above table.**

TESTING THE POCKELS CELL @ 633nm– OUTSIDE OF A LASER SYSTEM

These tests are usually performed for either a) inspection of a new or repaired Pockels cell, or b) determination of the proper operation of a Pockels cell. If the Pockels cell is in a laser system, please refer to that portion of the manual for proper setup.

Remove any protective end caps from the cell, and carefully visually inspect that the cell is clean and clear by looking through it. Double check the serial number against the data sheet provided to aid in setup the testing parameters.

Use two suitable polarizers, which are crossed polarized to each other. Let P1 be in the same polarization as the input laser beam. Use vertical polarization for the input laser beam. P1 can be eliminated if the test laser has a polarization ratio greater than 100:1.

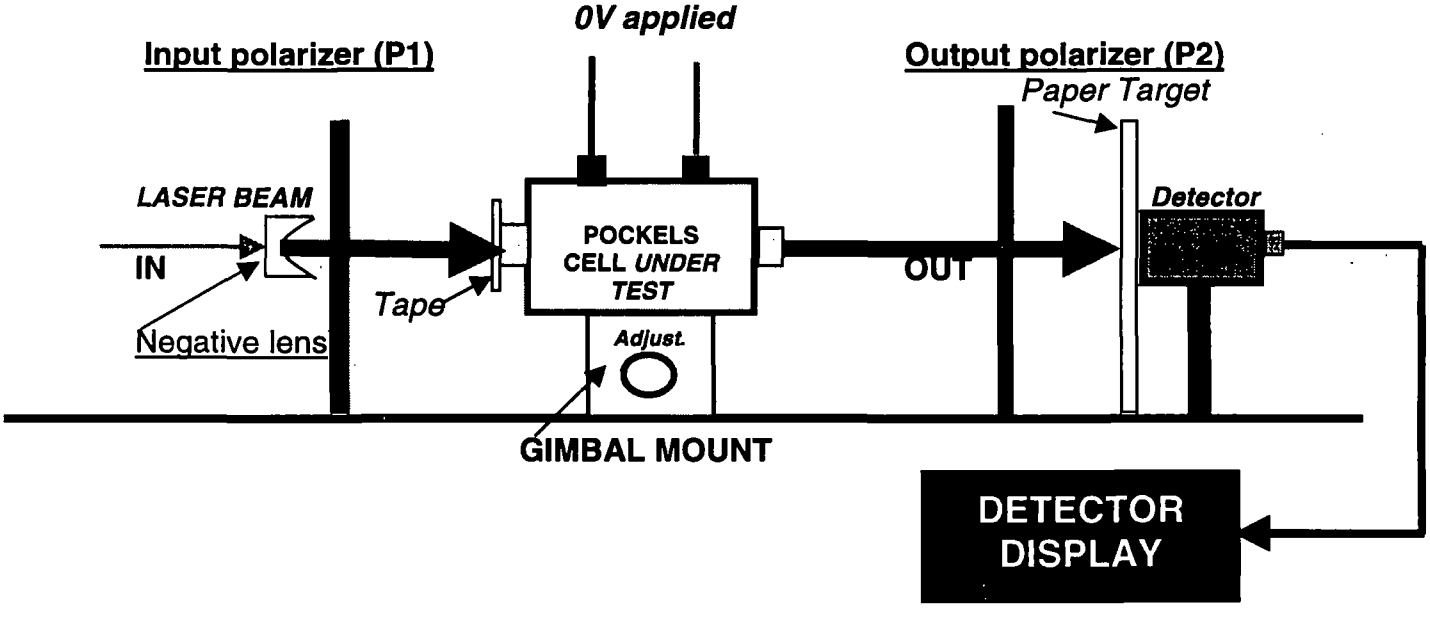
Set up the optical system as shown in figure 1.

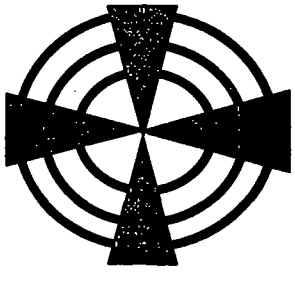
Make sure the high voltage power supply is OFF and discharged before connection to the Pockels cell.

This manual references a HeNe laser at 1 mW for these tests, and recommends this method. The detector and display must be able to clearly show the minimum and maximum changes in laser beam intensity. A photodiode (biased) and an oscilloscope works very well. A low light power meter for 633nm is acceptable also.

Align the optical system such that the laser beam goes through the center of the Pockels cell (bore sighted) and falls directly on the active portion of the detector. with P2 removed. Note – be assured that P2, if not a sheet polarizing filter, does not displace the beam appreciably on the detector. If it does, compensate for the deviation when necessary. When P2 is replaced, (make sure it is crossed to the input polarization), observe the detector display.

Place a piece of translucent material such as "invisible" Scotch tape or lens tissue before P1. It is also recommended that a negative lens be placed also before P1 (with the tape) to expand the beam for easy observation. Place a white cardboard or paper sheet (paper target) in from of the detector for visual observation of the pattern referred to as the "Maltese cross".



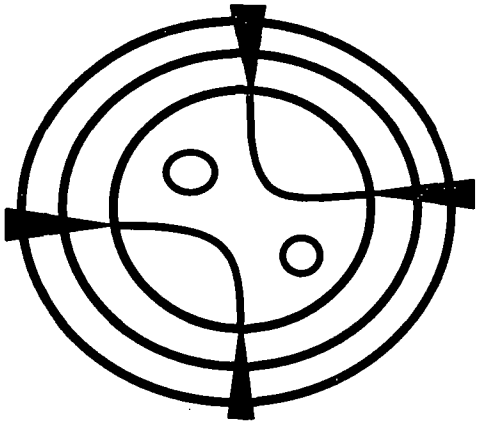


Ideal displayed cross

The paper target should show a projection as sketched here. The concentric circles should be as "round" as possible. The intersection of the cross must also be coincident with the laser beam that was bore sighted initially.

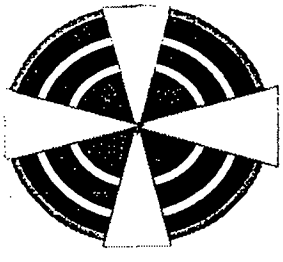
At this point the high voltage will be brought up to a value as shown in the data sheet sent with the Pockels cell. Increase the voltage slowly, and never exceed by 20% the value shown on the data sheet. While observing the paper target, increase the voltage until the cross opens, as shown in sketch.

This represents the pattern on the target paper at the halfwave voltage. The center opening should be clear.



Ideal sketch of Pockels cell pattern

Record the halfwave voltage at this point, but do not exceed ~ 15% of the data sheet voltage.
To obtain a better value for the halfwave voltage is to rotate P2 by 90-degrees, so that it in the same polarization plane as P1. At the halfwave voltage, a negative or inverse Maltese cross will be displayed. Remove the paper target and obtain a peak or maximum value on the display from the detector pickup. It should be less than 10% of that voltage value as recorded on the data sheet. Disconnect the Pockels cell from the High Voltage power supply, *after* the supply has been shutdown and discharged.



The inverted or negative image with P1 and P2 aligned to the polarization of the test laser. Compare to previous cross.

Ideal displayed negative or inverted cross

TRANSMISSION LOSS

It is recommended that this test be performed at the wavelength at which the Pockels cell is to be used, since other wavelengths will produce errors because of the AR coating lose. Use a power level between 1mW and 10mW.

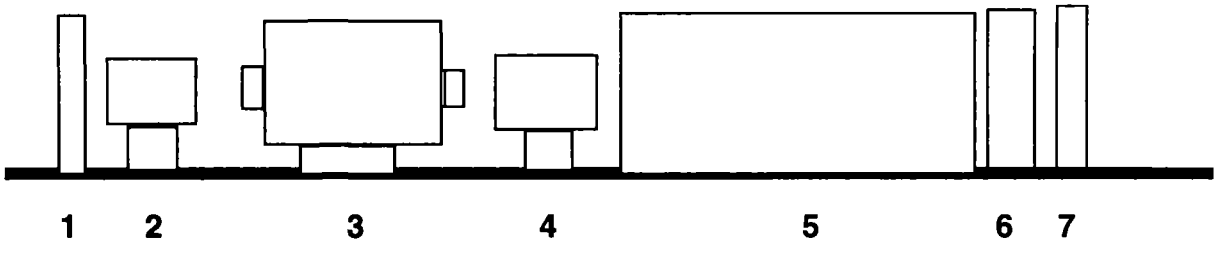
In this test, a laser power meter is required. Set the power to the proper conditions.

With the cell removed, measure the laser output power.

Without any polarizers, P1 and P2, and with the cell disconnected from the High Voltage Power Supply measure the output and record the power level from the display with the beam going through the center of the Pockels cell. Be careful to align the cell to the beam, so that it is bore sighted through the center of the cell. Measure the power, and calculate the loss. It should be 4~5% less.

NOTE: The previous test - TESTING THE POCKELS CELL @ 633nm– OUTSIDE OF A LASER SYSTEM – can be run at the actual wavelength, but keep the power low in CW mode. Sometimes this is not practical.

SETUP OF A POCKELS CELL OPRATING A QUARTERWAVE VOLTAGE UTILIZING A QUARTERWAVE PLATE IN A LASER CAVITY



Basic generic setup of a laser cavity

(For reference – there are many other configurations depending on application)

Where:

1 – Rear Mirror (Usually 1005 @ λ
2 – Quarterwave plate
3 – Pockels cell
4 – Polarizer (if necessary)
5 – Laser Head
6 – Shutter/Spatial filter
7 – Front mirror/output coupler

In this configuration the Pockels cell (See: **Basic generic setup of a laser cavity - sketch**) is operated in the quarterwave voltage (~ ½ of the halfwave voltage), and with no voltage applied to the cell until Q-switching is required. The Pockels cell used should have all ready been accepted as a working unit.

To setup the Pockels cell in an actual cavity, use a HeNe laser carefully aligned to the laser rod with all optical elements in place. Sometimes, it is easier to add one element at a time and adjust accordingly as other pieces are secured to the optical rail. Make certain that the laser system is OFF!

Defuse the HeNe laser (tape) and place target paper at the front mirror towards the laser head. Remove the shutter and spatial filter. Be assured that the "Maltese cross" is centered on the bore sighted He-Ne. With all elements replaced, the laser is ready for testing.

In simple terms, to obtain a GIANT pulse (Q-switched laser) two factors must be adjusted. The voltage on the Pockels cell which controls the polarization rotation, and the delay of the Q-switch trigger. The delay sets up the point at which the Pockels cell receives a signal allow to rotate the polarized light of the laser to create the GIANT pulse.

With the flash lamp ON, the population inversion takes place in the laser medium. However, the rear mirror is block because of the quarterwave plate. Since no voltage is across the Pockels cell the polarized light goes through the cell unaltered. The light gets rotated by the quarterwave plate, reflects off the rear mirror, returns again through the quarterwave plate, being rotated an again. When it reaches the polarizer it is orthogonal (90-degrees) or crossed to it, and the polarized light does not pass. Therefore, no lasing action. When a high voltage is applied to the Pockels cell at the quarterwave voltage, the light, which was unaltered before, now rotated by a quarterwave. Then passing through the quarterwave plate, it is rotated a complete halfwave, and is reflect back by the rear mirror. Entering the quarterwave plate and Pockels cell it is rotated again by halfwave. Now it passes through the polarizer, and lasing begins. Since the cavity was blocked, the lasing medium has built up greatly, and the sudden discharge of photons produce the GIANT pulse.

QUANTUM TECHNOLOGY, INC.
TEST DATA SHEET
Q-SWITCH

CUSTOMER :UNIV. OF CA., SAN DIEGO
MODEL : QS-3-2H
SERIAL NO : Q02-159
W/O NO : Q02-159

CRYSTAL PARAMETERS

MATERIAL	: BBO
APERTURE (mm.)	: 3
TERMINALS	: TT
HOUSING	: BLACK DELRIN
CUSTOMER DRAWING NO.	: NA.

OPTICAL QUALITY CONTROL

TRANSMISSION AT 1064nm.	: NA.
CONTRAST RATIO	: >1000:1
HALF-WAVE VOLTAGE @ 632.8 nm. (KV.)	: 2.0

PHYSICAL PARAMETERS
INDEX MATCHING FLUID: N2

AR COATING (nm.) :	WINDOWS	633-1064 INPUT	633-1064 OUTPUT
:	CRYSTAL	800 INPUT	800 OUTPUT

COMMENTS:

TESTED BY: _____ DATE: 8/7/2002

QUANTUM TECHNOLOGY, INC.

108 COMMERCE ST., SUITE 101, LAKE MARY, FLORIDA 32746

TELEPHONE: (407) 333-9348 FAX: (407) 333-9352
E-MAIL:STAFF@QUANTUMTECH.COM

CERTIFICATE OF COMPLIANCE

CUSTOMER NAME: University of California, San Diego

PURCHASE ORDER NUMBER : 10211621

MATERIAL DESCRIPTION : Pockels cell, Mount, Driver & Pulser

MODEL NUMBER : QS-3-2H, MTP-1000, HVP-5I-DIFF & HVP-525D-R-50K

SERIAL NUMBER : Q02-159, E02-159E, E02-159 & E02-159D

ITEM QUANTITY : 1 of ea.

COMMENTS:
Also shipping cables:MHV-PT-RG62-18"(qty.2), 5PIN DIN_5 DIN-3 COND-6'(qty.1), SHV-SHV-RG59-6'(qty.1), BNCM-BNCM-RG188-6'(2), AC Cord & Instruction Manual .

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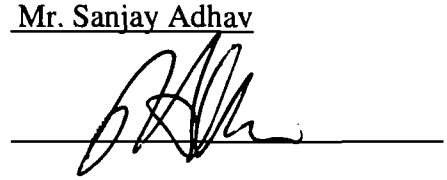
Mr. Sanjay Adhav



QUALITY ASSURANCE INSPECTOR DATE: August 26, 2002

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